Product Features

Operating Frequency: 30MHz ~ 1GHz

Gain Control: +13.5dB ~ +45dB

Minimum Gain Step: 0.5dB

Output Third-Order Interception: +34.2dBm

Vs=+5V (Bias Voltage)

V_{dd}=+5V (Supply Voltage)

Package: QFN32

Application

IF and RF Applications

Microcellular /3G Infrastructure

WiBro/WiMAX/4G

Microwave Radio and VSAT

Test Equipment with Sensors

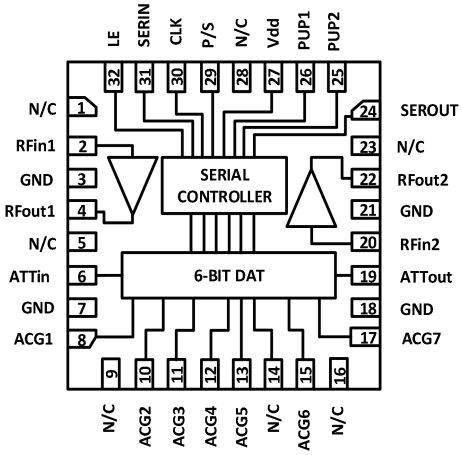
General Description

BR9032S is a digitally controlled variable gain amplifier which operates from 30MHz to 1GHz, and can be programmed to provide anywhere from 13.5dB to 45dB of gain, in 0.5 dB steps. The BR9032S delivers a noise figure of 1.8dB and an OIP3 of +34.2dBm in its maximum gain state. This single positive control line per bit digital attenuator incorporates off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Using different combinations of off-chip choke inductors and decoupling capacitors, the product can realize the electrical performance of different bands of frequencies and high integration in leadless surface-mount QFN32 package.

Ordering Information

Part Number	Package	Description
BR9032S	QFN32	30MHz~1GHz Variable Gain Amplifier

Functional Block Diagram



Technical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Gain (maximum gain state)	30MHz to 1GHz	44	44.7	45	dB
Attenuation range	30MHz to 1GHz	0.5	-	31.5	dB
Input Return Loss	30MHz to 1GHz	-	-22.9	-	dB
Output Return Loss	30MHz to 1GHz	-	-15.8	-	dB
Reverse Isolation	30MHz to 1GHz	-	-57	-	dB
Attenuation Accuracy: (Reference Insertion Loss)	30MHz to 1GHz 0.5dB to 31.5dB attenuation states	-0.1	-	+0.7	dB
Output Power for 1dB compression	30MHz to 1GHz	-	21.2	-	dBm
Output Third-Order Interception	30MHz ~ 1GHz	-	34.2	-	dBm
Noise figure	30MHz to 1GHz	-	1.8	-	dB
Switching features Trise (50% CTL-90% RF) Tfall (50% CTL-10% RF)	100MHz at 16dB attenuation state	 - -	 105 419	 - -	 ns ns
Supply voltage	-	-	5	-	V
Supply Current	-	-	130	-	mA
Test Conditions: Vs=V_{dd}=+5V, V_{ctl}=0V/5V, I=130mA, OIP3 spacing=1MHz, Pout=+5dBm/tone, Temp=+25℃					

Absolute Maximum Ratings

RF Input Power: -10dBm (T=+85 ° C)

Control Voltage Range: -0.5V ~ +5.5V

Maximum Bias Voltage (Vs): +5.5V

Maximum Operating Voltage (V_{dd}): +5.5V

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

Recommended Operating Conditions

Bias Voltage (Vs): 5V

Supply Voltage (V_{dd}): 5V

Switching Voltage: 0V ~ 0.8V (Low Level)

2.7V ~ Vdd (High Level)

PUP1/PUP2 Control Voltage:

0 ~ 0.8V (Low Level)

Vdd-0.5 ~ Vdd (High Level)

Supply Current: 130mA

Operating Temperature: -55℃ ~ +125℃

Storage Temperature: -65℃ ~ +150℃

ESD WARNING

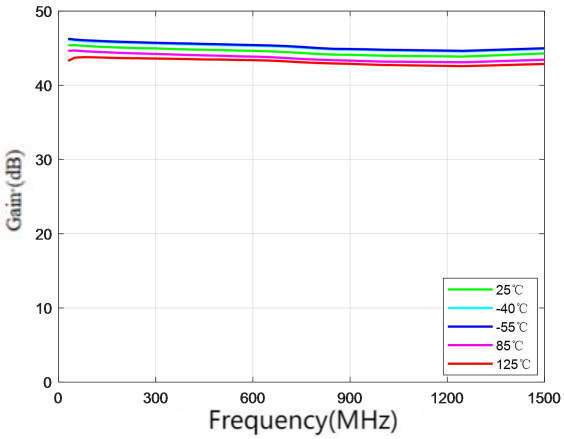
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

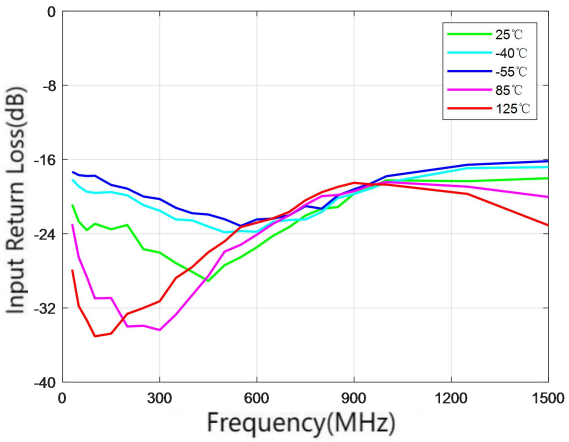
Typical Performance (EVB test results)

Parameters	Typ.											Units
Frequency	10	20	30	50	75	100	150	200	250	300	350	MHz
Gain	45.4	45.4	45.4	45.4	45.3	45.2	45.1	45.1	45.0	45.0	44.9	dB
Input Return Loss	-20.3	-20.5	-20.8	-22.7	-23.6	-22.9	-23.5	-23.1	-25.7	-26.0	-27.2	dB
Output Return Loss	-12.4	-12.2	-12.1	-12.0	-11.9	-11.7	-12.1	-12.1	-13.3	-14.0	-15.0	dB
Reverse Isolation	-53.1	-54.0	-54.5	-54.4	-55.2	-55.3	-56.2	-54.1	-54.7	-55.6	-57.1	dB
Output Power for 1dB compression	19.3	20.4	20.5	20.7	21.0	21.1	21.1	21.1	21.2	21.1	21.1	dBm
Output Third-Order Interception	36.2	34.0	34.1	35.2	35.3	34.7	35.4	34.1	35.2	33.7	34.6	dBm
Noise Figure	-	-	2.0	1.8	1.8	1.8	1.7	1.7	1.8	1.7	1.7	dB
Frequency	400	450	500	550	600	700	800	850	900	950	1000	MHz
Gain	44.8	44.8	44.8	44.7	44.6	44.5	44.2	44.1	44.1	44.0	44.0	dB
Input Return Loss	-28.1	-29.1	-27.4	-26.5	-25.4	-23.3	-21.3	-21.1	-19.7	-19.1	-18.2	dB
Output Return Loss	-15.8	-16.9	-18.2	-20.1	-20.1	-20.3	-18.6	-17.8	-16.4	-15.9	-15.2	dB
Reverse isolation	-55.9	-56.4	-57.4	-57.6	-55.9	-56.6	-54.3	-55.0	-56.9	-57.9	-54.7	dB
Output Power for 1dB compression	21.1	21.3	21.3	21.4	21.4	21.2	21.3	21.3	21.5	21.4	21.6	dBm
Output Third-Order Interception	34.1	33.6	34.5	33.2	33.0	32.5	31.8	32.5	32.1	32.3	32.3	dBm
Noise Figure	1.7	1.7	1.7	1.8	1.7	1.8	1.8	1.8	1.8	1.8	1.8	dB

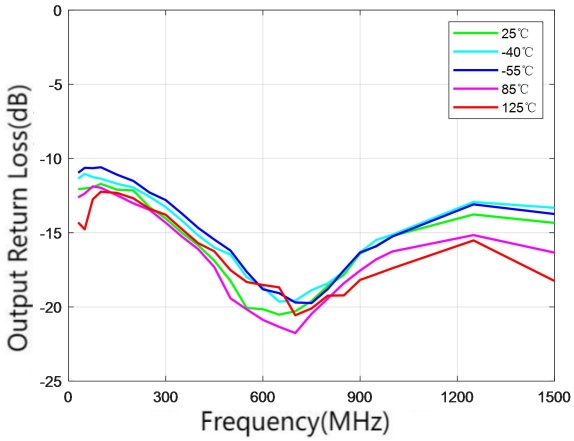
Test Conditions: Vs=V_{dd}=+5V, I=130mA, OIP3 spacing=1MHz, Pout=5dBm/tone; TA=+25℃



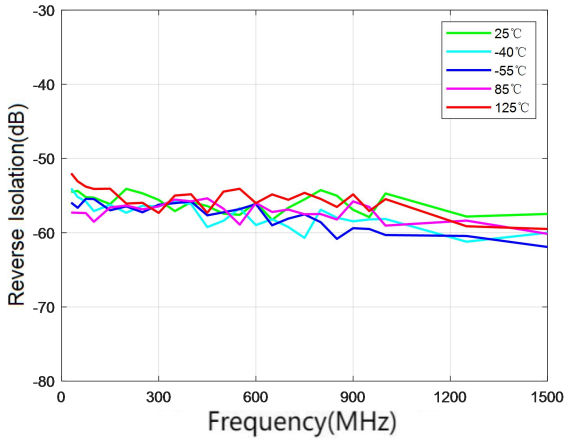
Gain



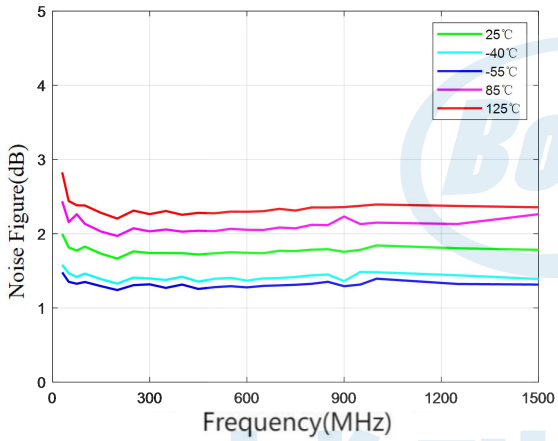
Input Return Loss



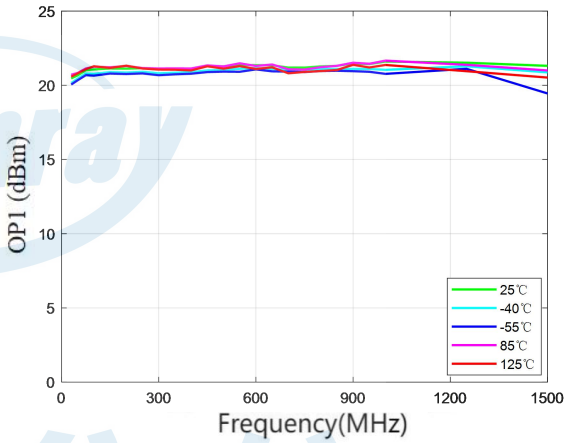
Output Return Loss



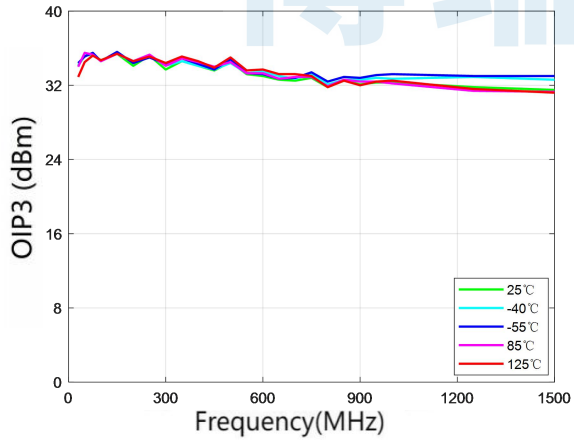
Reverse Isolation



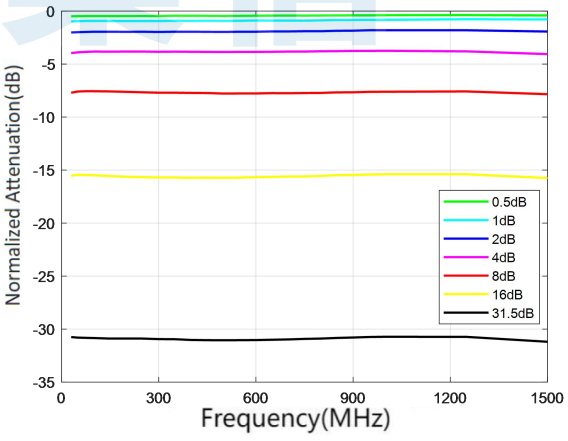
Noise Figure



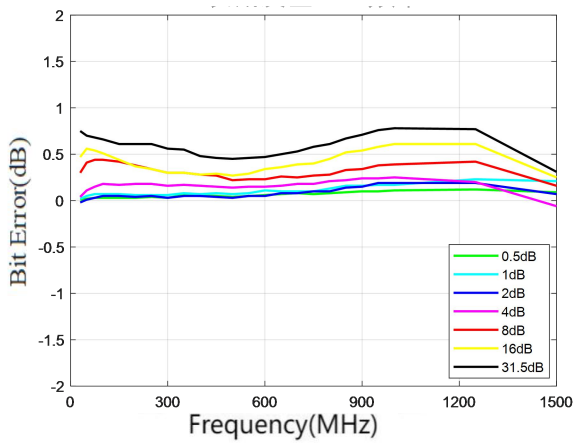
Output Power for 1dB Compression



Output Third-Order Interception

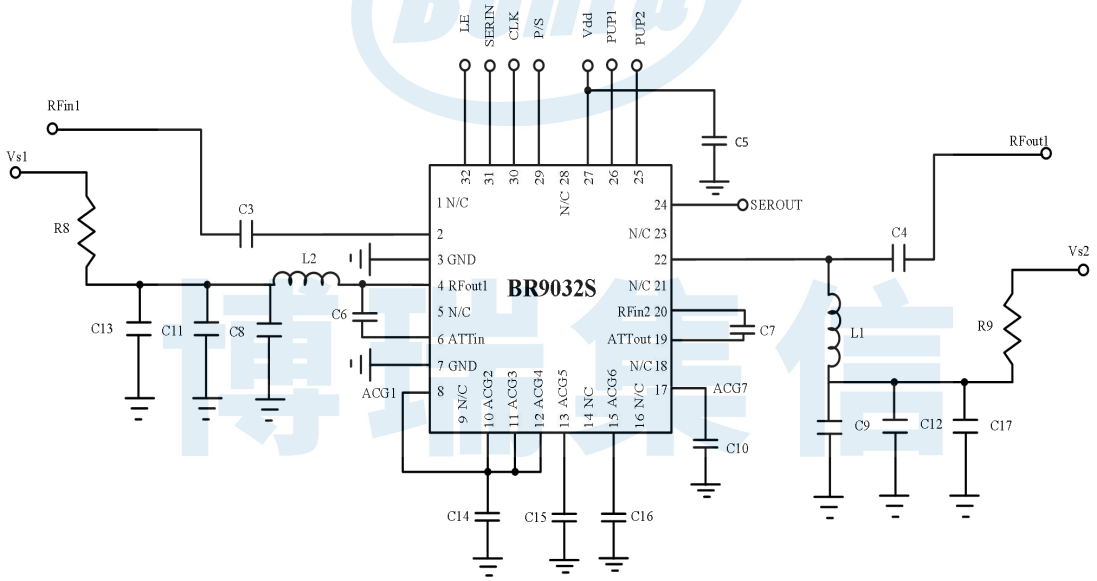


Normalized Attenuation



Bit Error

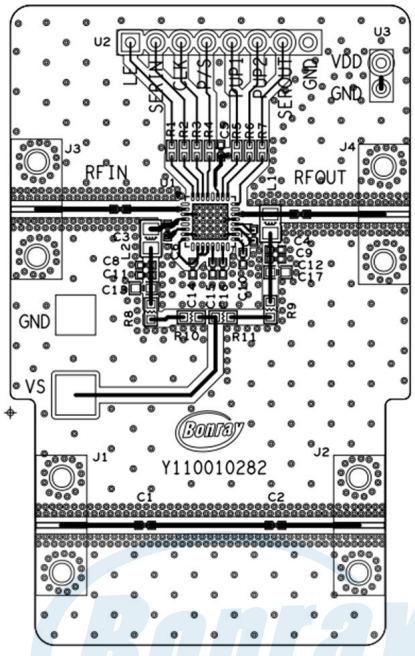
Typical Application Schematic



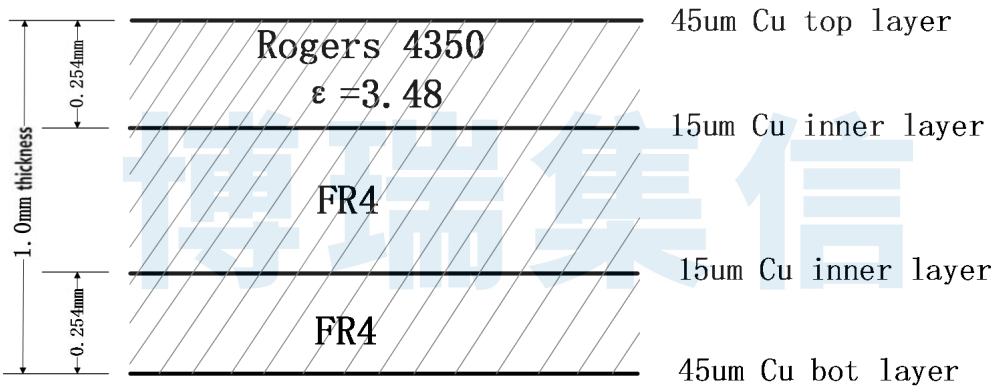
Bill of Material

Designator	Package	Description	Part Number
C3 to C7, C10 to C12, C14 to C16	0402	1000pF	GCM155R71H102KA37D
C8, C9	0402	100pF	GRM1555C1H101JA01D
L1, L2	0805	1.5 uH	0603AF-152XJEW
R8, R9	0402	0 Ω	RC0402FR-070RL

PCB Evaluation Board

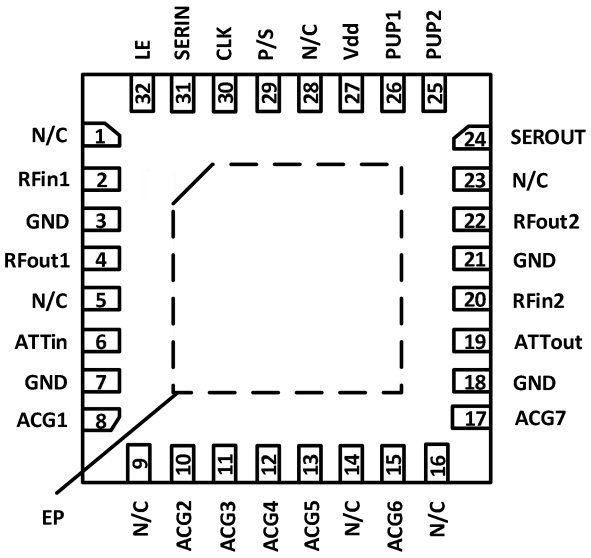


PCB



50 ohms Impedance Signal Lines： width=0.53mm, spacing=0.53mm

Pin Configuration and Description



Pin Number	Pin Name	Description	
1,5,9,14,16,23,28	N/C	No electrical connection. Provide grounded land pads for PCB mounting integrity.	
2,20	RFin1, RFin2	Amplifier input pins. DC Block is required.	
4, 22	RFout1, RFout2	Amplifiers output and DC bias pins, External bias tee is required.	
3,7,18,21	GND	RF/DC ground pins. Connect to ground.	
6, 12	ATTin, ATTout	Attenuator RF Input/Output. DC block is required.	
8,10,11,12,13,15,17	ACG1 ~ ACG7	AC grounding capacitor pins. External capacitors to ground are recommended. Place capacitor as close to pins as possible.	
24	SEROUT	Serial interface data output pin. Serial input data is delayed by six clock cycles.	See Truth Tables and serial control interface diagram
25, 26	PUP2, PUP1	Power-up state selection pins.	
30	CLK	Serial interface clock input pin.	
31	SERIN	Serial interface data input pin.	
32	LE	Latch enable input pin.	
29	P/S	Parallel/Serial mode selection pin.	
27	Vdd	Power supply pin.	
-	EP	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistant; see PCB Mounting Pattern for suggested footprint.	

Power-Up State

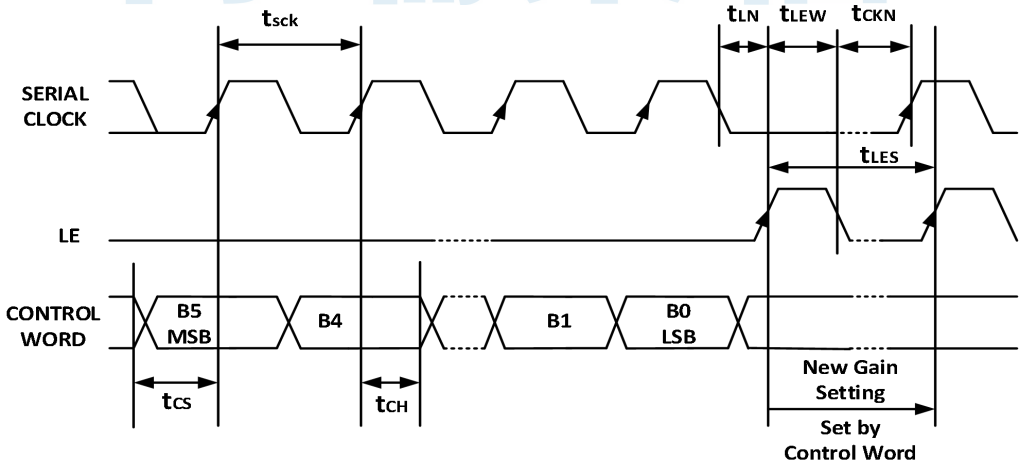
If the LE is set to logical LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table.

PUP Truth Table

LE	PUP1	PUP2	Relative Attenuation Setting
0	0	0	-31.5 dB
0	1	0	-24dB
0	0	1	-16dB
0	1	1	Insertion Loss

Serial Control Interface

The BR9032S contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). It is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches were used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading. For all modes of operations, gain will remain constant while LE is kept low.



Timing Specifications Table

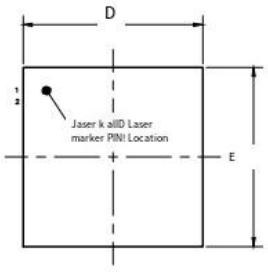
Serial Number	Parameters	Typ.	Serial Number	Parameters	Typ.
1	Minimum clock period (tSCK)	100ns	5	Minimum LE pulse duration (tLEW)	10ns
2	Control signal setup time (tCS)	20ns	6	Minimum LE pulse interval time (tLES)	630ns
3	Control signal hold time (tCH)	20ns	7	Serial clock hold time (tCKN) from LE	10ns
4	LE signal setup time (tLN)	10ns			

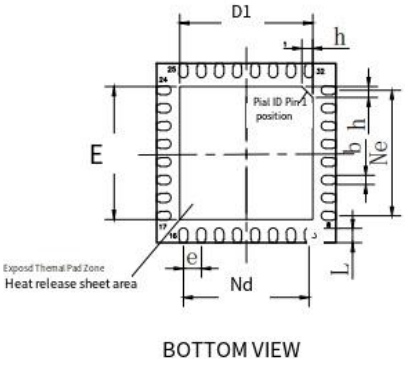
Serial Control Truth Table

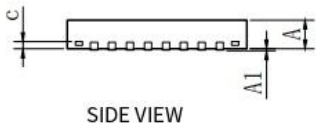
Serial Control Words						Relative Attenuation Setting
B5 16dB	B4 8dB	B3 4dB	B2 2dB	B1 1dB	B0 0.5 dB	
1	1	1	1	1	1	Reference 0dB
1	1	1	1	1	0	-0.5dB
1	1	1	1	0	1	-1dB
1	1	1	0	1	1	-2dB
1	1	0	1	1	1	-4dB
1	0	1	1	1	1	-8dB
0	1	1	1	1	1	-16dB
0	0	0	0	0	0	-31.5dB

Note: Any combination of the above states provides an attenuation approximately equal to the sum of the bits selected.

Package Dimensions (mm)







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	4.90	5.00	5.10
D1	3.35	3.40	3.45
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E1	3.35	3.40	3.45
L	0.35	0.40	0.45
h	0.25	0.30	0.35