Product Features

Operating Frequency: 2GHz ~ 20GHz

Gain: 15dB@11GHz

Noise Figure: 2.1dB@11GHz

Output Power for 1dB Compression:

16.6dBm@11GHz

Output Third-Order Interception:

25.4dBm@11GHz

Supply Current:48mA@ Vdd=+5V

23mA@ Vdd=+3.3V

Die Size: 2.7×1.5×0.1(mm)

Application

Radar and Electronic Countermeasures

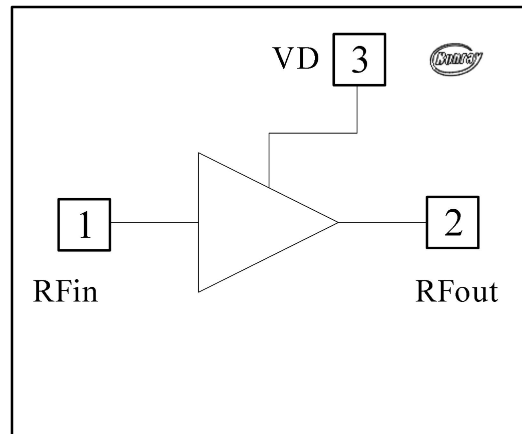
Military and Aerospace

Test Instrumentation

General Description

BR9643LDZ is a MMIC gain block amplifier die designed using GaAs process which operates between 2GHz~20GHz. The amplifier is powered by a single-supply operation of +5V or +3.3V. At 11GHz, the amplifier typically provides a gain of 15dB, an output P1dB of 16.6dBm, and a noise figure of 2.1dB under the condition of +5V power supply. It has been internally matched to 50 ohms and AC coupled, thereby eliminating the need for external DC blocks and RF port matching. The BR9643LDZ amplifier is ideal for integration into Multi-Chip-Modules (MCMs) due to its small size.

Functional Block Diagram



Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Gain	2000MHz	-	16	-	dB
	11000MHz	-	15	-	dB
	20000MHz	-	13.8	-	dB
Output Power for 1dB Compression	4000MHz	-	18.5	-	dBm
	11000MHz	-	16.6	-	dBm
Output Third-Order Interception	4000MHz	-	26.8	-	dBm
	11000MHz	-	25.4	-	dBm
Noise Figure	11000MHz	-	2.1	-	dB
Input Return Loss	11000MHz	-	-21	-	dB
Output Return Loss	11000MHz	-	-21.2	-	dB
Reverse Isolation	11000MHz	-	-34.2	-	dB
Supply Voltage	-	-	5	-	V
Supply Current	-	-	48	-	mA
Test Conditions: Vdd=+5V, Idd=48mA, OIP3 spacing=1MHz, Pout=0dBm/tone, TA=+25℃					

Absolute Maximum Ratings

Maximum Operating Voltage : +6V

Maximum RF input Power: +15dBm

Recommended Operating Conditions

Supply Voltage: +5V/+3.3V

Supply Current: 48mA@+5V; 23mA@+3.3V

Operating Temperature: -55℃ ~ +125℃

Storage Temperature: -65℃ ~ +150℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability.

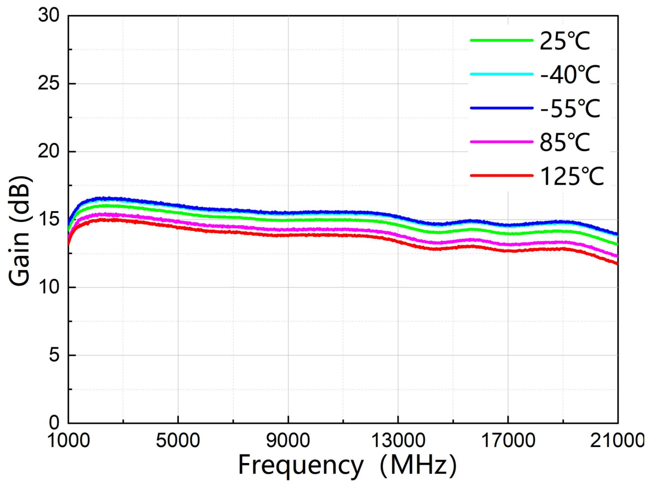
ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

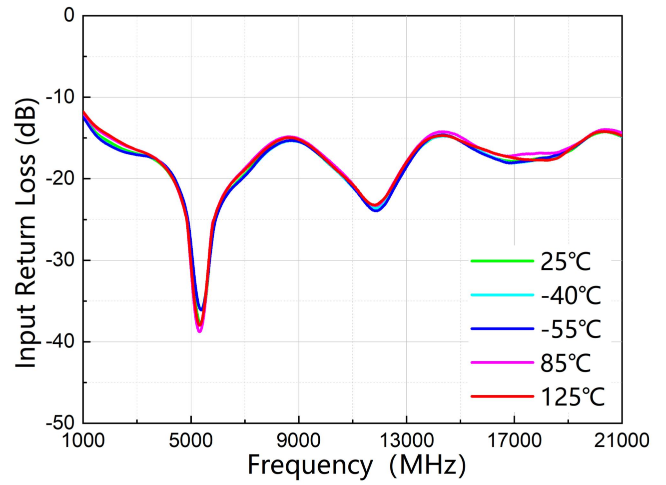
OBSERVE HANDLING PRECAUTIONS

Typical Performance (Probe test results at +5V supply voltage）

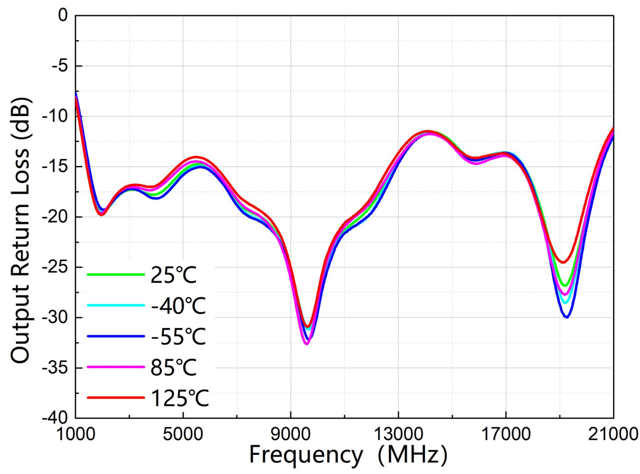
Parameters	Typ.											Units
Frequency	1000	2000	3000	4000	5000	6000	7000	8000	9000	10000	11000	MHz
Gain	14.1	16	16	15.7	15.2	15.2	15.2	15	15	15	15	dB
Input Return Loss	-12.1	-15.5	-17	-18.5	-27.9	-24.2	-19.4	-16.2	-15.4	-17.8	-21	dB
Output Return Loss	-7.8	-19.5	-17.4	-17.8	-15.5	-15.1	-18.5	-20.3	-24.5	-28.8	-21.2	dB
Reverse Isolation	-33.1	-30.8	-30.2	-30.3	-31.2	-32.2	-33.3	-33.8	-34.9	-34	-34.2	dB
Output Power for 1dB Compression	15.2	17.7	17.8	18.5	18.2	18.2	17.5	16.9	16.9	16.6	16.6	dBm
Output Third-Order Interception	24	26.5	27.1	26.8	26.5	26.4	26	25.9	25.4	25.6	25.4	dBm
Noise Figure	3.1	3.1	2.7	2.5	2.4	2.3	2.2	2	2	2	2.1	dB
Frequency	12000	13000	14000	15000	16000	17000	18000	19000	20000	21000	22000	MHz
Gain	14.9	14.6	14.1	14.1	14.2	14	14.1	14.1	13.8	13.2	12.7	dB
Input Return Loss	-23	-18.6	-15	-15.4	-17	-17.9	-17.4	-16.7	-14.4	-14.8	-17.4	dB
Output Return Loss	-19	-14.4	-11.7	-12.5	-14.2	-13.5	-16.9	-26.2	-19.7	-11.6	-10	dB
Reverse Isolation	-34.8	-35.4	-38.6	-38.3	-38.9	-42	-41.2	-38.9	-38.7	-38.3	-40.4	dB
Output Power for 1dB Compression	16.3	16.1	14.6	13.5	12.7	12.3	12.5	11.8	12.3	11.4	10.3	dBm
Output Third-Order Interception	25.1	24.8	24	23.3	22.9	22.4	22.2	22	21.5	20.5	19.9	dBm
Noise Figure	2.3	2.5	2.7	2.7	2.6	2.6	2.7	3	3.2	3.4	3.4	dB
Test Conditions: Vdd=+5V, Idd=48mA; OIP3 spacing=1MHz, Pout=0dBm/tone; TA=+25℃												



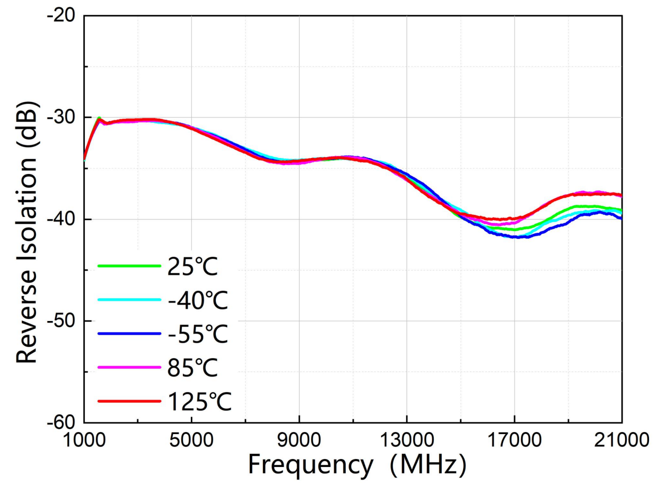
Gain vs. Freq



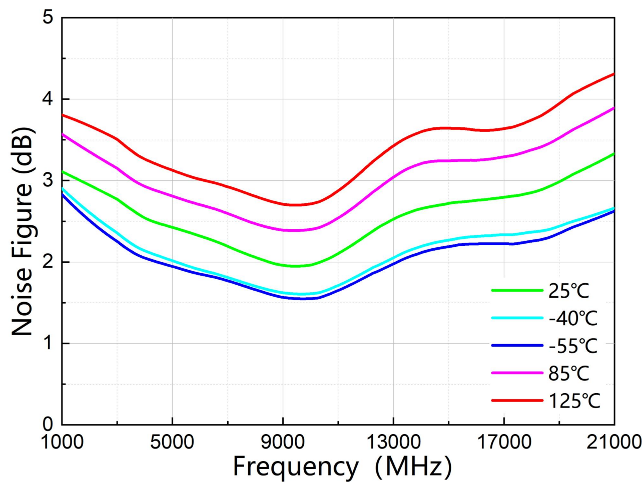
Input Return Loss vs. Freq



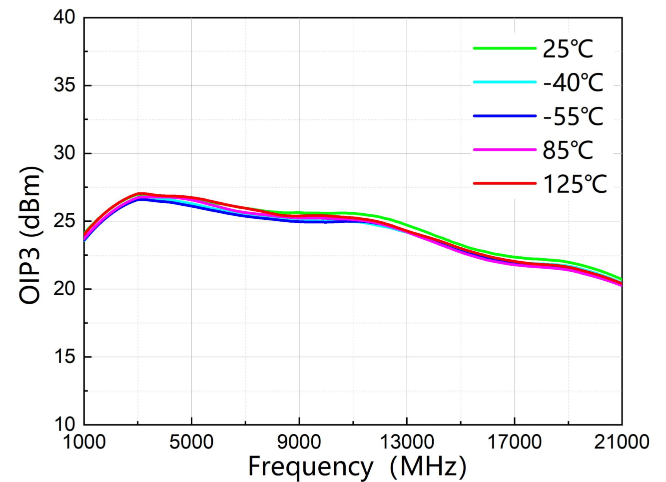
Output Return Loss vs. Freq



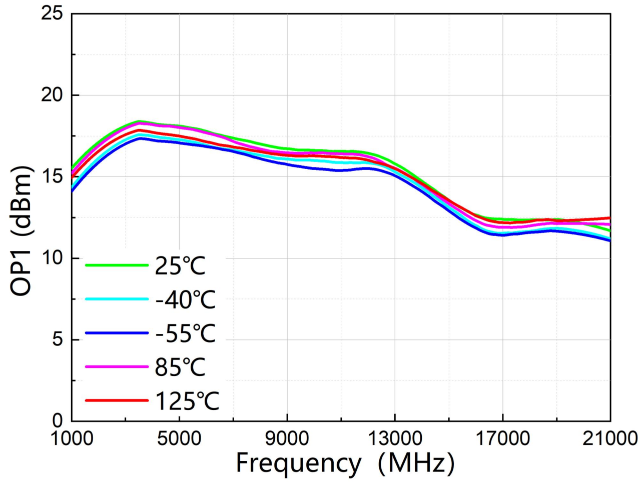
Reverse Isolation vs. Freq



Noise Figure vs. Freq



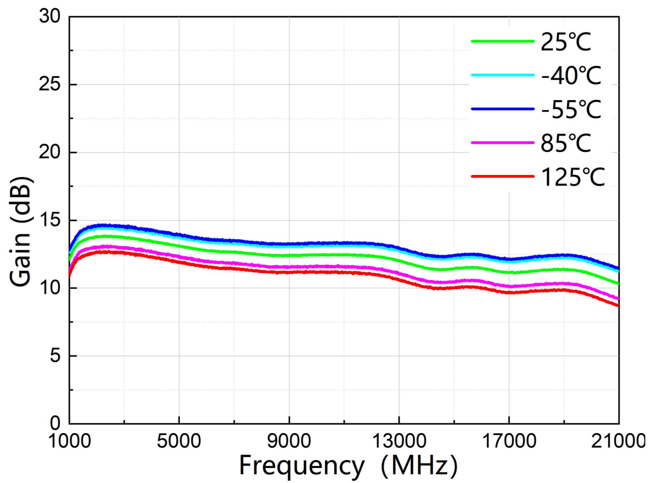
Output Third-Order Interception vs. Freq



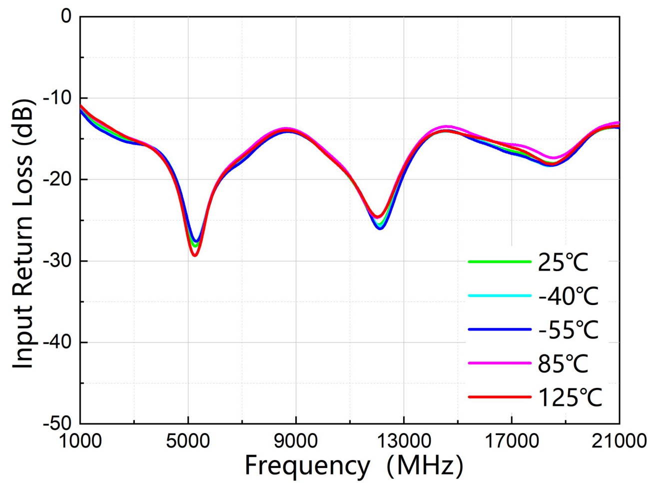
Output Power for 1dB Compression vs. Freq

Typical Performance (Probe test results at +3.3V supply voltage）

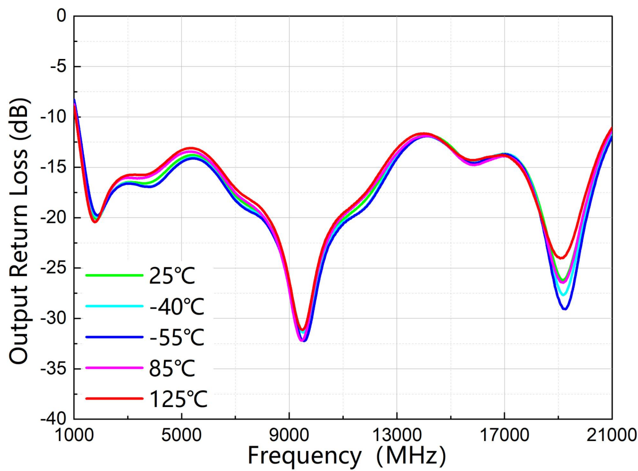
Parameters	Typ.											Units
Frequency	1000	2000	3000	4000	5000	6000	7000	8000	9000	10000	11000	MHz
Gain	12.1	13.7	13.7	13.4	12.8	12.4	12.2	12.5	11.9	12	12	dB
Input Return Loss	-11.2	-14	-15.4	-17.1	-25.9	-21.2	-17.4	-14.9	-14.2	-16.5	-20.1	dB
Output Return Loss	-8.5	-19.4	-16.6	-16.3	-14.1	-14.4	-17.7	-19.9	-26.1	-26.5	-20.1	dB
Reverse Isolation	-31.7	-30.3	-30.2	-30.4	-31.4	-33.2	-34.2	-33.5	-32.8	-32.8	-33.6	dB
Output Power for 1dB Compression	14.3	15.7	16.5	16.3	16.4	16.4	15.5	15.3	15.3	15.6	15.7	dBm
Output Third-Order Interception	22.6	23.5	23.6	24.1	24	23.8	23.6	23.5	23.4	23.2	23.4	dBm
Noise Figure	2.8	3.3	2.9	2.7	2.7	2.6	2.6	2.5	2.4	2.4	2.5	dB
Frequency	12000	13000	14000	15000	16000	17000	18000	19000	20000	21000	22000	MHz
Gain	11.8	11.4	11.5	11.4	11.5	11.1	11.3	11.4	11.1	9.5	9.9	dB
Input Return Loss	-25.2	-19.2	-14.7	-14.3	-15.4	-16.4	-17.7	-17.5	-14.3	-13.7	-15.1	dB
Output Return Loss	-17.6	-13.9	-11.9	-13	-14.7	-13.6	-16.6	-25.6	-19.4	-11.5	-9.8	dB
Reverse Isolation	-33.2	-34	-35.9	-35.6	-33.9	-34.8	-33.1	-31.5	-31.9	-32.2	-31.1	dB
Output Power for 1dB Compression	15.8	14.6	14.2	9.9	6.8	7.5	6.9	8.6	11.4	11.2	14.5	dBm
Output Third-Order Interception	23.3	23.2	22.7	20.6	19	18.8	18.1	17.7	17.7	17.5	16.8	dBm
Noise Figure	2.7	3.1	3.2	3.3	3.3	3.1	3.2	3.5	3.6	3.7	3.6	dB
Test conditions: Vdd=+3.3V, Idd=23mA; OIP3 spacing=1MHz, Pout=5dBm/tone; TA=+25℃												



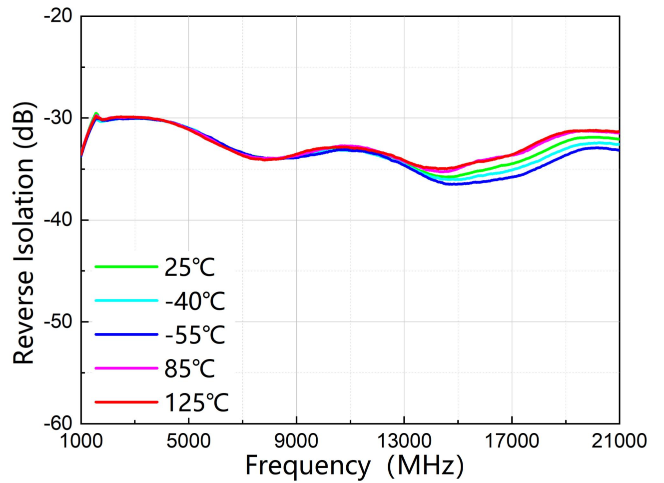
Gain vs. Freq



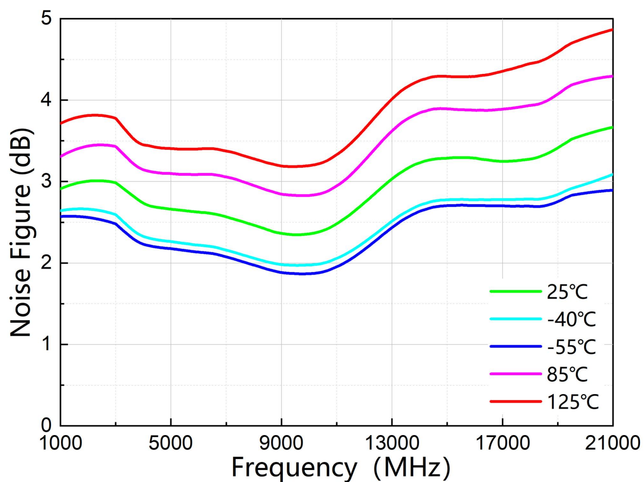
Input Return Loss vs. Freq



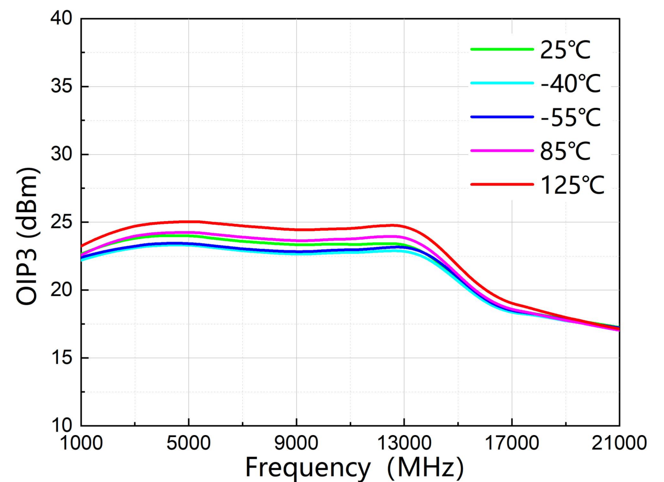
Output Return Loss vs. Freq



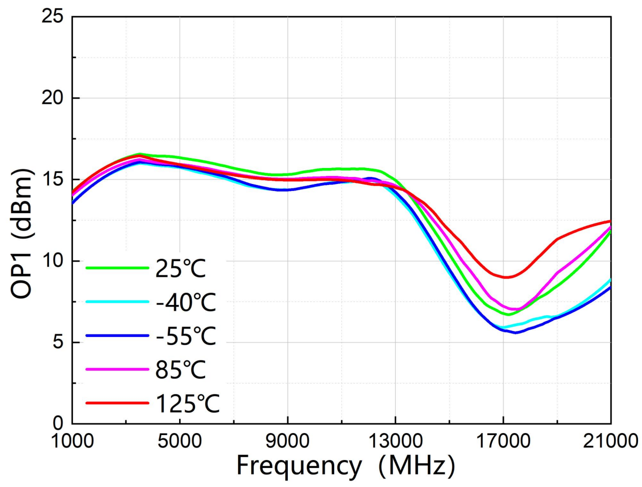
Reverse Isolation vs. Freq



Noise Figure vs. Freq

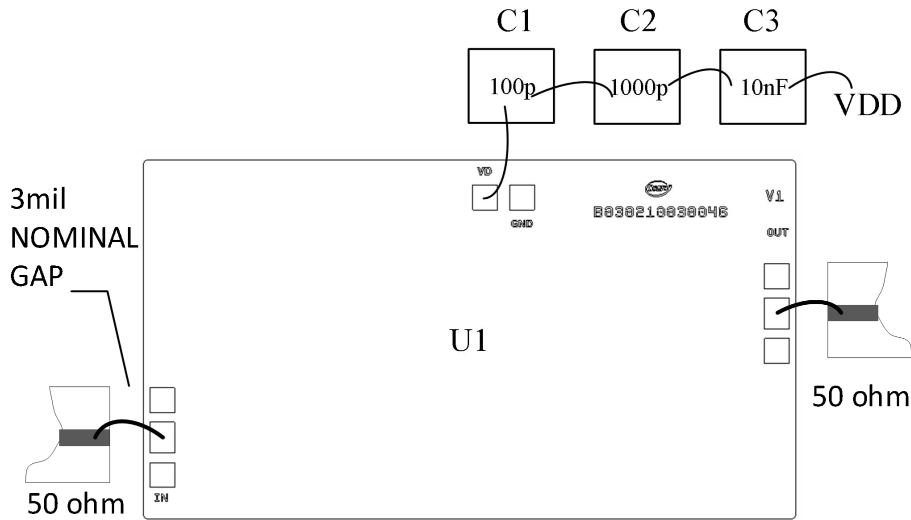


Output Third-Order Interception vs. Freq



Output Power for 1dB Compression vs. Freq

Assembly Diagram



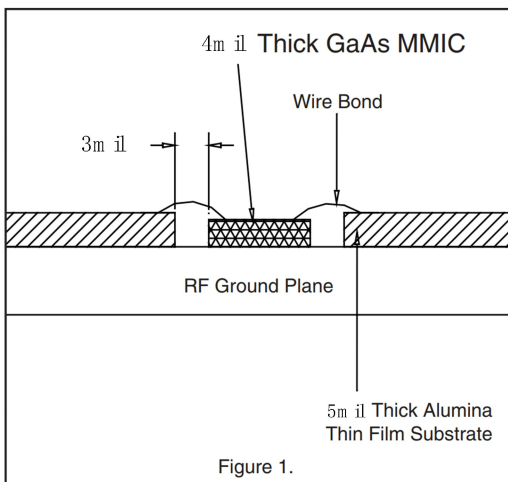


Figure 1.

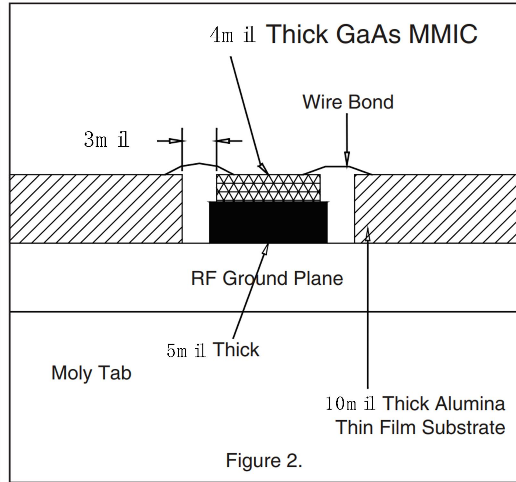


Figure 2.

Note: Chip capacitors as close as possible to power supply pad

Bill of Material

Reference Designator	Package Size	Value	P/N
U1	Naked Die	2GHz~20GHz	BR9643LDZ
C1	Chip Capacitor	100pF	SG201N101MSTW
C2	Chip Capacitor	1000pF	CT91202X102M100TW
C3	Chip Capacitor	10nF	CT91-20-2X-103-M-50-C-W

Handling Precautions:

1. **Storage:** All bare dies are placed in ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

2. Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

3. Electrostatic protection: Follow ESD precautions to protect against ESD strikes.

4. Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pickup.

5. General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip should not be touched with vacuum collet, tweezers, or fingers.

6. Mouning: The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

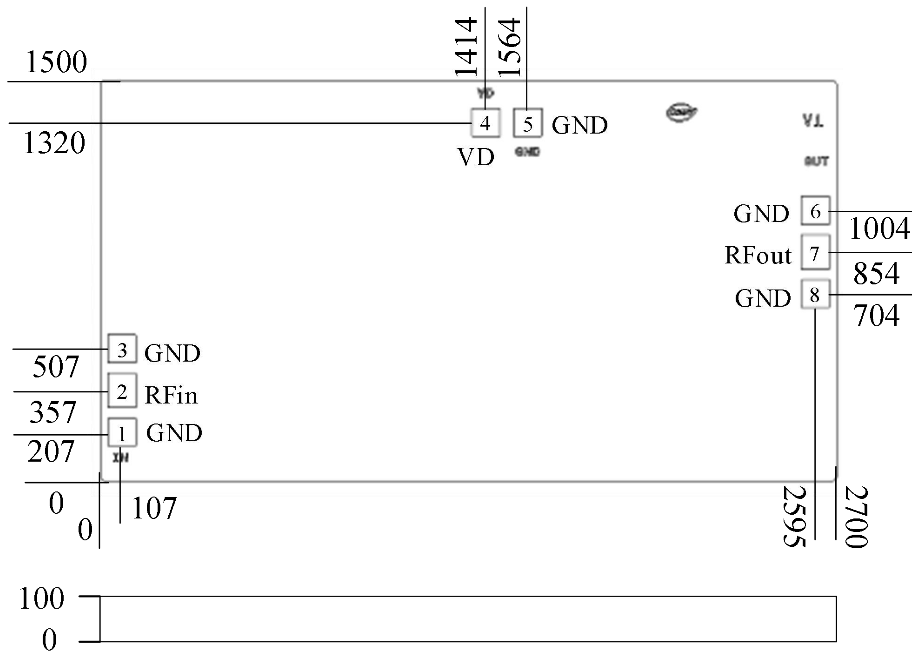
7. Conductive epoxy Die Attach: Apply conductive epoxy to the mounting surface so that the overflow of conductive epoxy on all four sides should not be less than 75%, and the height of conductive epoxy climbing on all four sides should not exceed the surface of the chip. Cure conductive epoxy per the manufacturer's schedule

8. Bonding process: Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. **The length of all bonds should be as short as possible and the arc height as low as possible.**

9. Die bonding void rate: not more than 10%.

10. Please contact customer service if you have any problem.

Mechanical Information (Units: mm)



Notes:

1. Backside and bond pad metal: Gold;
2. Backside is RF and DC ground;
3. Pad size: RFin 100um×125um; RFout 100um×125um; VD 100um×100um;
4. Cannot be bonded on the hole.

Pad Description

Pad Number	Pad	Function Description
2	RFin	RF Input, matched to 50 Ohms and AC coupled.
7	RFout	RF Output, matched to 50 Ohms and AC coupled.
4	VD	Power Supply. See assembly for required external components.
1, 3, 5, 6, 8	GND	Connected to the bottom of die through hole
Die Bottom	GND	Die bottom must be well grounded to RF/DC