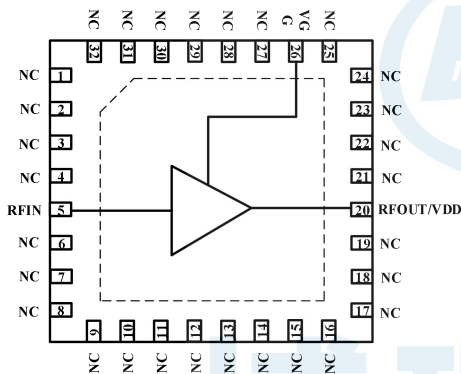


**Product Features**

- Frequency: 10MHz ~ 1GHz
- Gain : 20.8dB@500MHz
- Psat: 40.3dBm@500MHz
- PAE: 59.9%(500MHz)
- Supply Voltage: 28V,  $I_{DQ}$  70mA
- Package: QFN32 (5mm×5mm)

**General Description**

The BRGF010010FLJ is a gallium nitride (GaN) Internal Matched power amplifier that achieves 10W (40dBm) output with a power PAE of 59.9% ( $P_{out}=40.3dBm$ , 500MHz) over an instantaneous bandwidth of 10MHz to 1GHz. The product is ideal for pulsed or continuous wave Application, such as radar, public mobile radio communications, and general-purpose amplification technologies.

**Functional Block Diagram**

**Ordering Information**

Part Number	Package	Description
BRGF010010FLJ	QFN32	10 MHz to 1GHz 10W Internal Matched PA

**Absolute Maximum Ratings**

Parameters	Values
Gate Drain Breakdown Voltage ( $BV_{DG}$ )	100V
Gate Voltage Range ( $V_{GG}$ )	-6 to 0V
Drain Current ( $I_D$ )	1.3 A
Gate Current ( $I_G$ )	5mA
Continuous Dissipated Power ( $P_D$ )	20.3 W.
Channel Temperature ( $T_{CH}$ )	275 °C
Mounting Temperature (30 seconds)	245 °C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

**Recommended Operating Conditions**

Parameters	Values
Drain Voltage ( $V_{DD}$ )	+28V (Typ)
Drain Static Current ( $I_{DQ}$ )	70mA (Typ)
Gate Voltage ( $V_{GG}$ )	-2.4V (Typ)
Storage Temperature	-65°C ~ +150°C
Operating Temperature	-55°C ~ +85°C

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

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**Impedance Mismatch**

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: EVB test,  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=+28\text{V}$ ,  
 $I_{DQ}=70\text{mA}$ ,  $F_{re}=1\text{GHz}$ , CW wave,  $P_{out}=10\text{W}$ .

**Thermal Parameters**

Parameters	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ )	DC at 85 ° C case	12.3	$^{\circ}\text{C}/\text{W}$
Channel Temperature ( $T_{ch}$ )		225	$^{\circ}\text{C}$

Note:  $\theta_{JC}$  to measure the thermal resistance to the bottom of the package

**ESD WARNING**

**ELECTROSTATIC SENSITIVE DEVICE**  
**OBSERVE HANDLING PRECAUTIONS**

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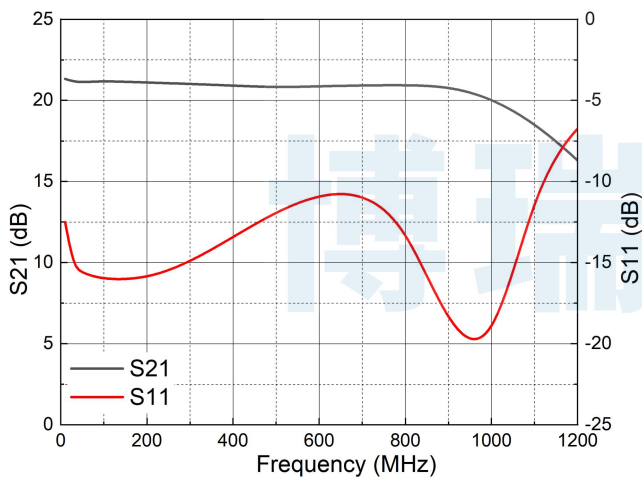
Typical Performanc (EVB test data,0.01GHz ~ 1GHz)

Parameters	Typ.										Units
	10	30	100	300	400	500	600	800	1000		
Frequency	10	30	100	300	400	500	600	800	1000		MHz
Gain	21.32	21.16	21.20	21.02	20.92	20.80	20.87	20.95	20.15		dB
Input Return Loss	-12.50	-15.27	-16.06	-14.97	-13.43	-11.85	-10.77	-12.58	-20.97		dB
Output Return Loss	-14.95	-20.95	-21.23	-17.49	-16.40	-15.56	-14.71	-15.61	-10.35		dB
Drain Current @P <sub>sat</sub>	546	457	472	521	544	616	712	778	590		mA
Pout ( dBm ) @P <sub>sat</sub>	39.60	39.42	39.66	39.94	40.15	40.26	40.94	41.81	40.47		dBm
PAE@P <sub>sat</sub>	57.01	65.61	67.58	65.35	65.99	59.85	60.00	67.54	65.33		%
Power Gain@P <sub>sat</sub>	13.53	13.92	14.66	14.76	15.38	15.58	14.37	15.21	15.02		dB

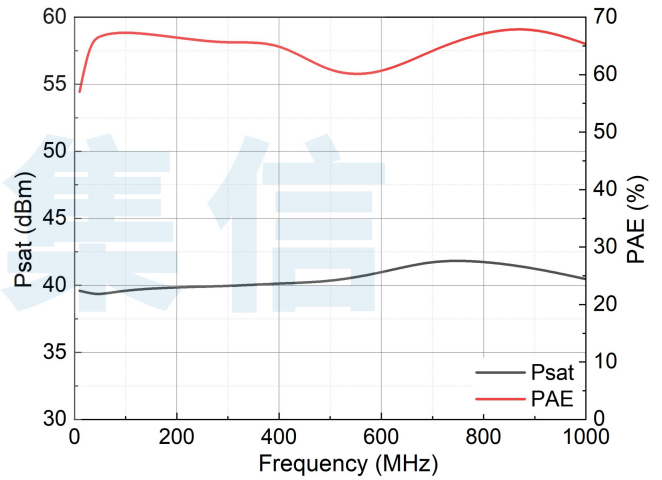
Test Condition: Temp =+25 ° C, V<sub>DD</sub>=+28V, I<sub>DQ</sub>=70mA

Note: P<sub>sat</sub> defined as the saturation power output of the evaluation board;

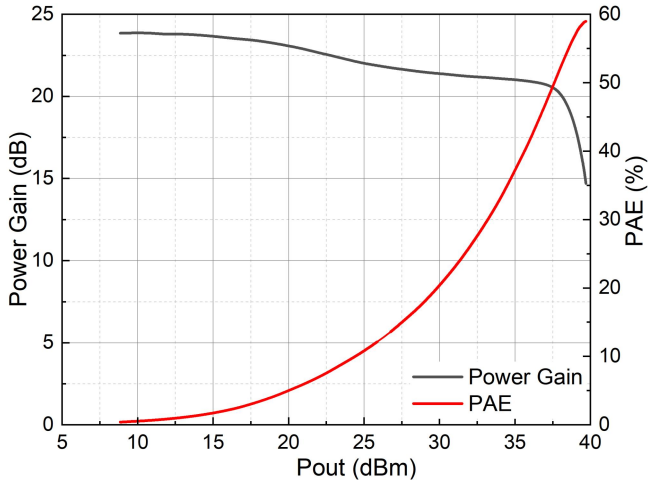
Typical Performanc (EVB test results)



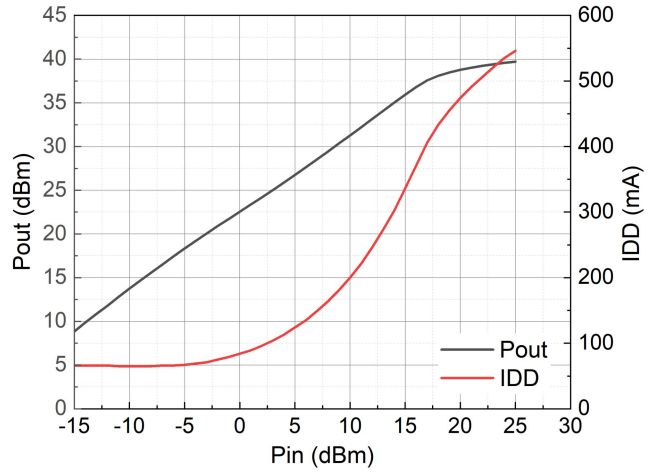
Gain , Input Return Loss vs. Freq



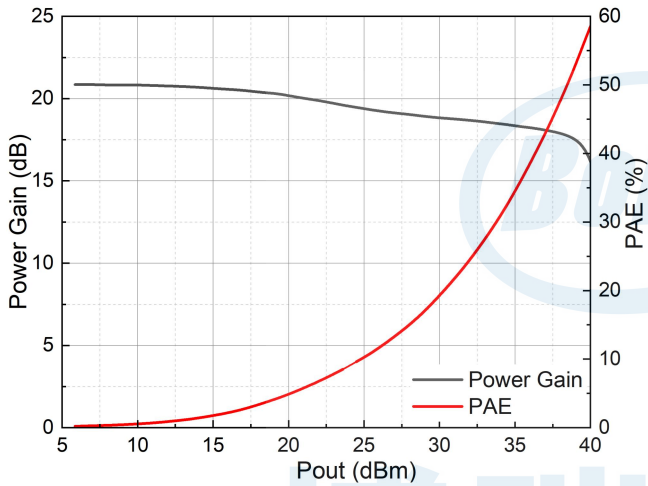
Psat, PAE vs. Freq



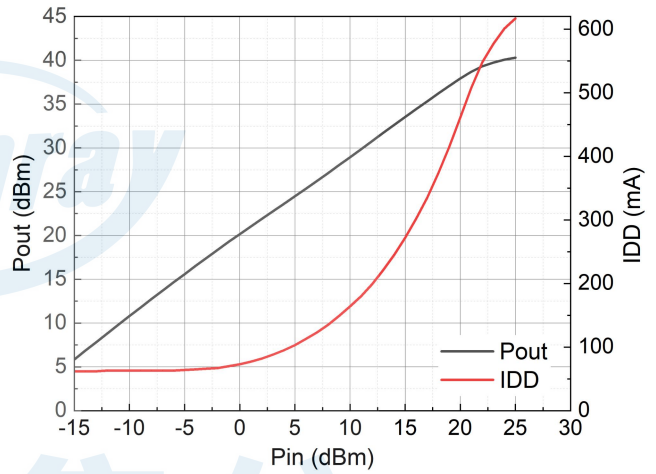
Gain, PAE vs. P<sub>out</sub> @10MHz



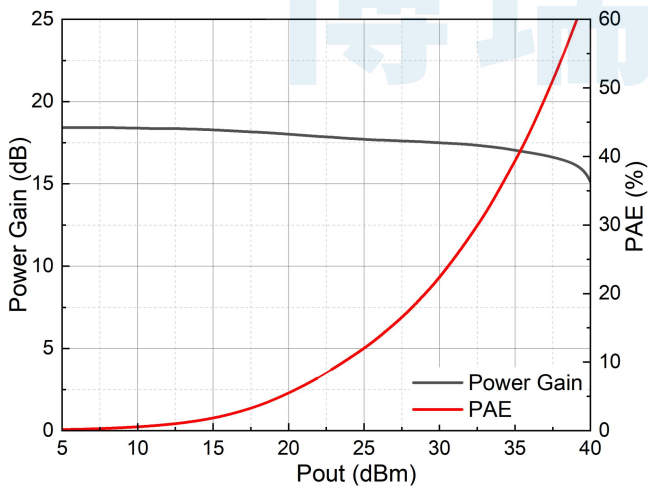
P<sub>out</sub>, IDD vs P<sub>in</sub> @10MHz



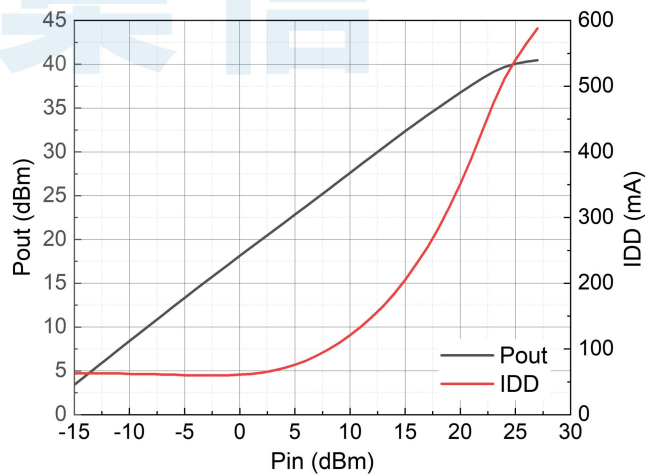
Gain, PAE vs. P<sub>out</sub> @500MHz



P<sub>out</sub>, IDD vs P<sub>in</sub> @500MHz

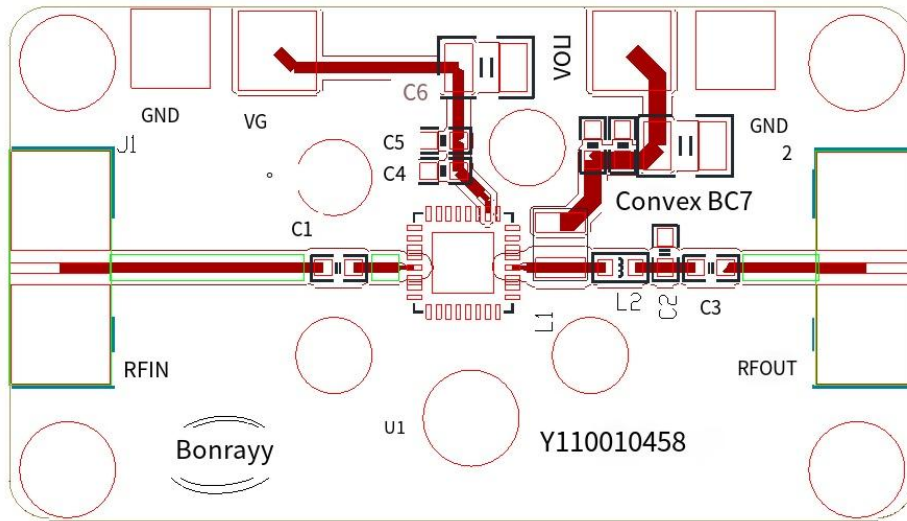


Gain, PAE vs. P<sub>out</sub> @1GHz

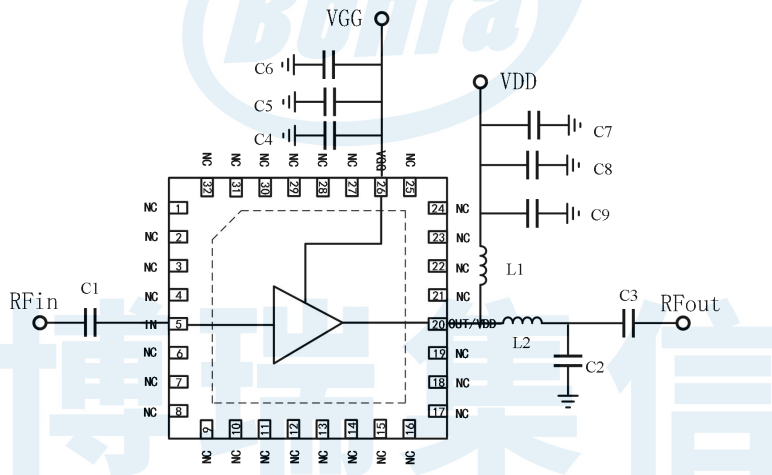


P<sub>out</sub>, IDD vs P<sub>in</sub> @1GHz

PCB Evaluation Board



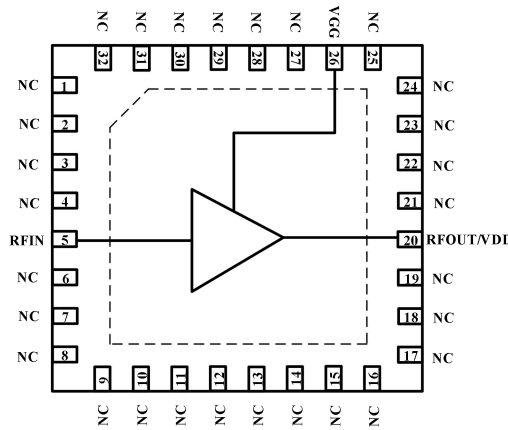
Typical Application Schematic



Bill of Material

Designator	Description	Part Number
L1	1.1 uH	1008AF-112XJRB
L2	6.2 nH	LQG18HH6N2S00D
C6, C7	10uF	GRM32ER71H106KA12L
C5, C8	100nF	GRM155R71H104KE14D
C4, C9	1nF	GRM188R71H102KA93D
C1, C3	2.2 nF	GRM1885C1H222JA01D
C2	2.4 PF	GQM1875C2E2R4BB12#

Pin Configuration and Description



Pin Number	Pin Name	Description
1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 30, 31, 32	NC	No internal connection, but connected to RF/DC ground when testing and using.
5	RFIN	RF input pins.
20	RFOUT/V <sub>DD</sub>	RF output and drain Supply Voltage voltage pins.
26	V <sub>G</sub>	Gate Supply Voltage voltage

Power-on sequence

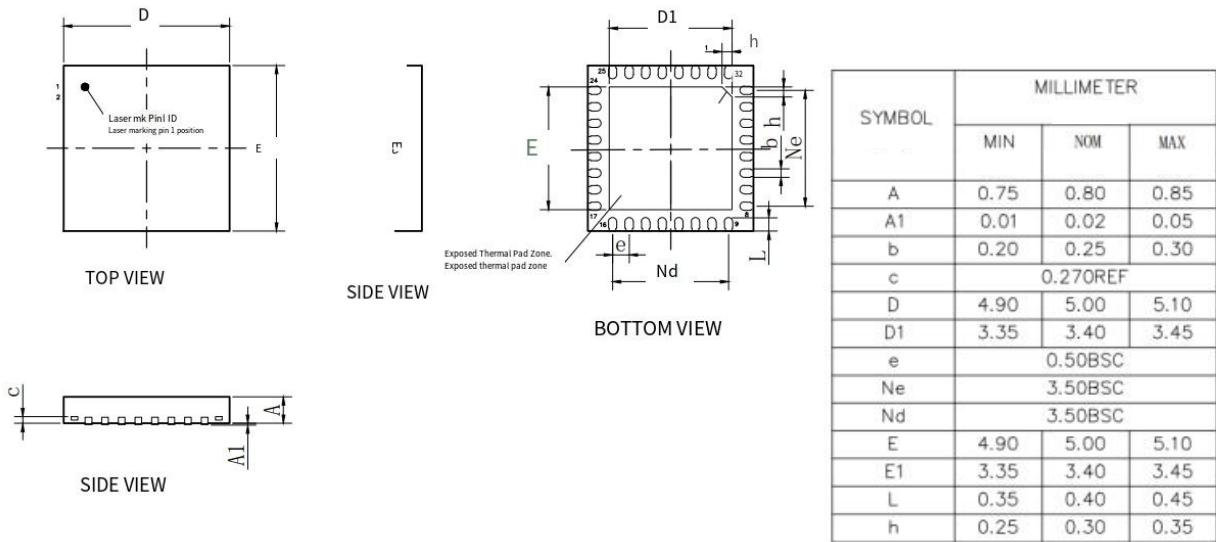
1. Set the gate voltage ( $V_{GG}$ ) to -5V
2. Set drain voltage ( $V_{DD}$ ) to +28V, current limit 500mA;
3. Open the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage ( $V_{GG}$ ) so that the drain current is 70mA;
6. Input RF signal;

Power-off sequence

1. Turn off the RF signal;
2. Reduce the gate voltage ( $V_{GG}$ ) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that  $V_{GG}$  is fully powered up before  $V_{DD}$  is applied, and that  $V_{DD}$  is lowered to below 5V before  $V_{GG}$  is powered down, especially in  $T_{DD}$  applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Recommended Soldering Temperature Profile

