Product Features

Frequency: 0.01GHz ~ 1GHz

Gain: 21.6dB@500MHz

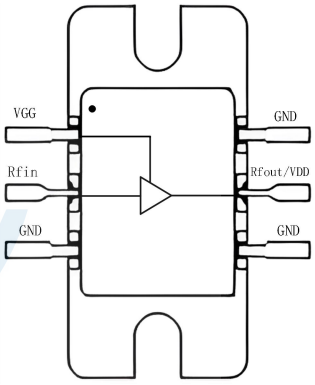
Psat: 40.0dBm@500MHz

PAE: 60.6%@500MHz

Operation Voltage: 28V, I_{DQ} 70mA

Package: PH (metal package)

Functional Block Diagram



General Description

BRGF010010PHG is a Gallium nitride (GaN) broadband power amplifier, the device achieves 10W (40dBm) output operating from 0.01GHz ~ 1GHz, Power added efficiency (PAE) up to 65%, small signal gain flatness of 4dB，using +28V drain power supply, quiescen current 70mA. BRGF010010PHG is ideal for pulse or continuous-wave applications such as wireless infrastructure, radar, public mobile radio communications, and general-purpose amplification technologies.

Ordering Information

Part Number	Package	Description
BRGF010010PHG	PH	10 MHZ to 1GHz 10W Internal Matched PA

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	1.4 A
Gate Current (I_G)	4mA
Continuous Dissipated Power (P_D)	25.8 W.
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Numerical values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	70mA (Typ)
Gate Voltage (V_{GG})	-2.46V (Typ)
Channel Temperature (T_{CH})	225 ° C (25 ° C)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Condition: EVB test, T_A=25℃, V_{DD}=+28V, I_{DQ}=70mA, Fre=1GHz, CW wave, P_{out}=10W test.

Thermal Parameters

Parameters	Test Condition	Value	Units
Thermal Resistance (θ_{JC})	DC at 85 ° C case	9.7	℃/W
Channel Temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

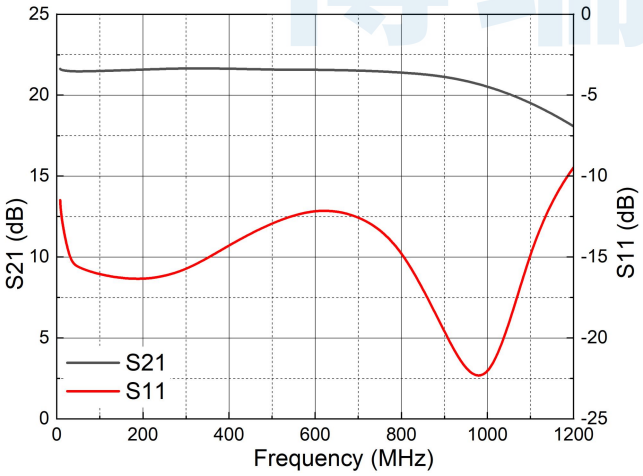
Typical Performanc (EVB test data, 0.01GHz ~ 1GHz)

Parameters	Typ.									Units
Frequency	10	30	100	300	400	500	600	800	1000	MHz
Gain	21.55	21.48	21.49	21.67	21.64	21.57	21.57	21.41	20.59	dB
Input Return Loss	-12.56	-15.30	-16.12	-15.89	-14.25	-12.85	-11.97	-14.18	-24.66	dB
Output Return Loss	-14.96	-19.24	-18.85	-18.22	-18.47	-18.93	-17.76	-14.07	-9.50	dB
Drain Current @P_{sat}	0.578	0.452	0.476	0.482	0.518	0.579	0.612	0.681	0.616	A
Output Power @P_{sat}	39.32	39.02	39.43	39.43	39.82	40.03	40.32	41.1	40.41	dBm
PAE@P_{sat}	50.55	59.46	62.97	63.12	63.86	60.59	60.81	65.59	61.91	%
Power Gain @P_{sat}	13.65	12.44	13.67	15.42	14.62	16.10	14.95	15.34	15.46	dB

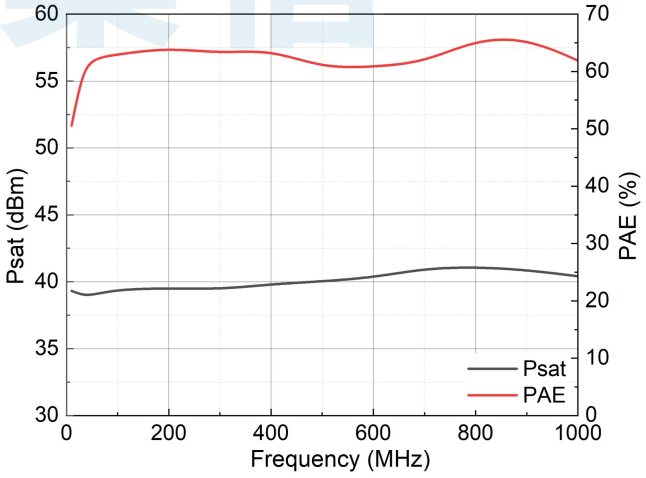
Test Condition: Temp =+25 ° C, V_{DD}=+28V, I_{DQ}=70mA

Note: P_{sat} defined as the saturation power output of the evaluation board;

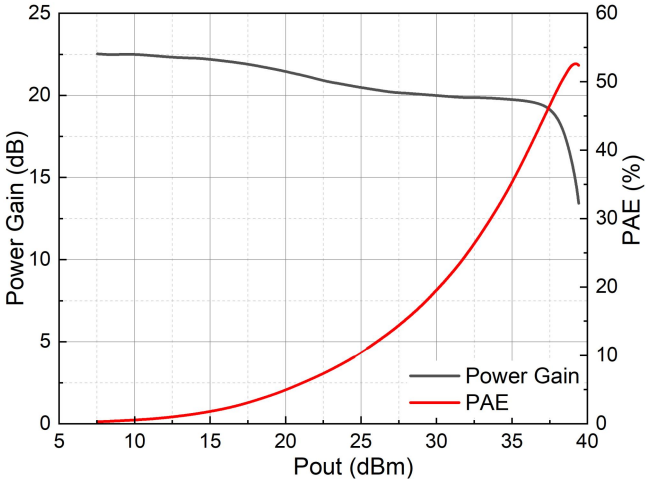
Typical Performanc (EVB test results)



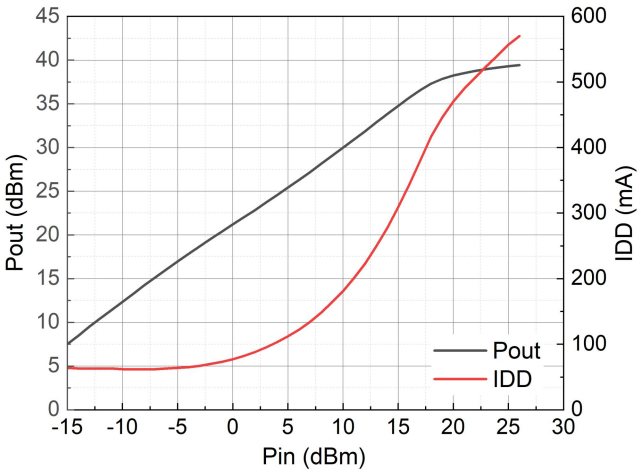
Input Return Loss, Gain vs. Freq



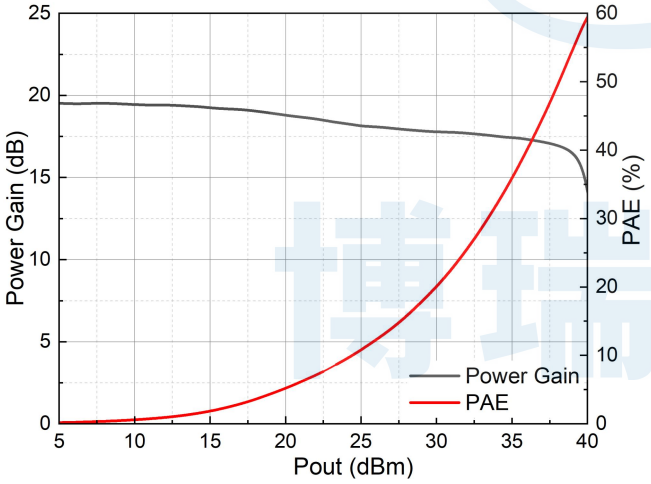
Psat, PAE vs. Freq



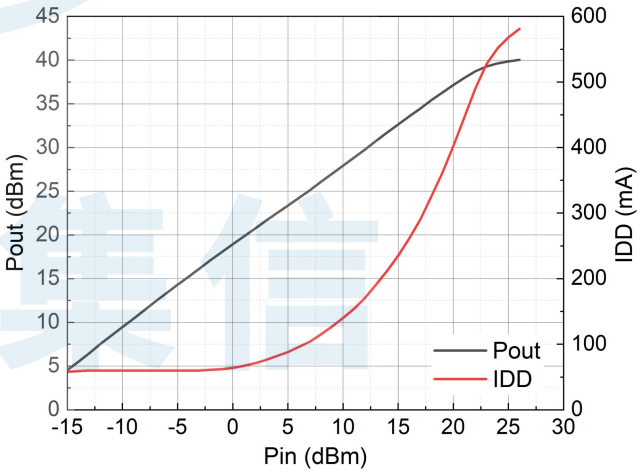
Gain , PAE vs. P_{out} @10MHz



P_{out} , IDD vs P_{in} @10MHz

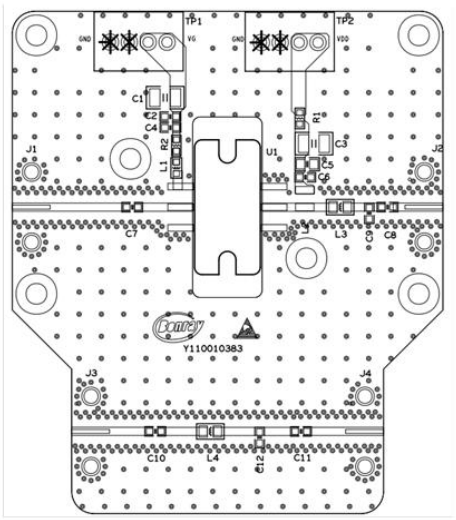


Gain , PAE vs. P_{out} @500MHz

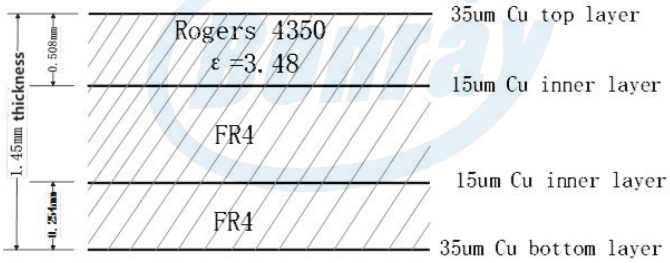


P_{out} , IDD vs P_{in} @500MHz

PCB Evaluation Board

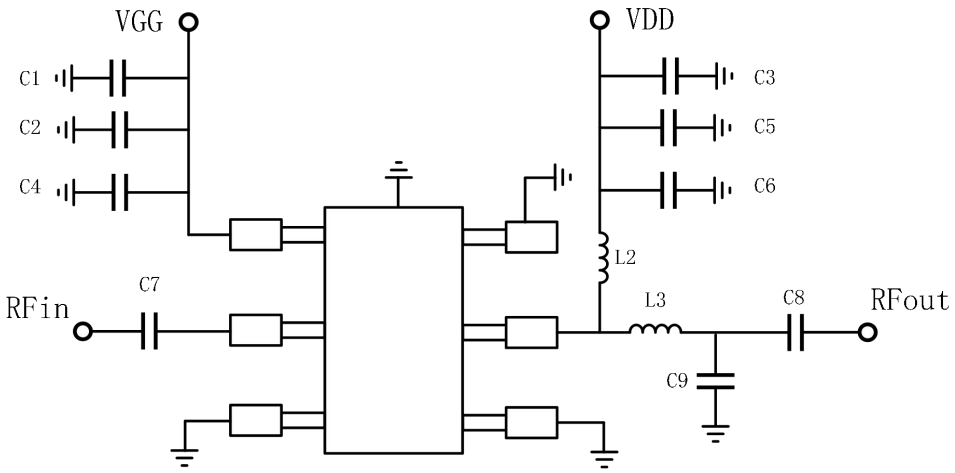


PCB



50 ohms Impedance Signal Lines： width=1.1mm, spacing=1.1mm

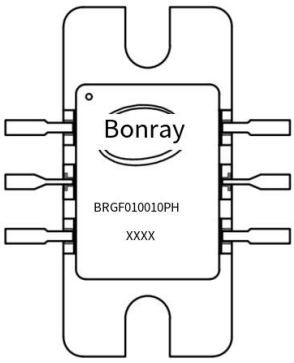
Typical Application



Bill of Material

Designator	Package	Description	Part Number
C1,C3	1210	10uF	GRM32ER71H106KA12L
C2,C5	0402	100nF	GRM155R71H104KE14D
C4,C6	0603	1nF	GRM188R71H102KA93D
C7,C8	0603	2.2 the nF	GRM1885C1H222JA01D
C9	0402	2.2 pF	GRM1555C1H2R2CA01D
L2	1008	1.1 uH	1008AF-112XJRB
L3	0402	4.7 nH	0402DC-4N7XJRU

Pin Configuration and Description



Pin Number	Pin Name	Description
1	VGG	Gate voltage
2	RFin	The pin is an RF signal input and requires an off-chip isolation capacitor.
Three minus	GND	Ground pins; This pin and the package substrate must be connected to the RF/DC ground.
5	RFout/VDD	Drain voltage / The RF signal of the amplifier output stage and the DC bias voltage supply the pins

Power-on Sequence

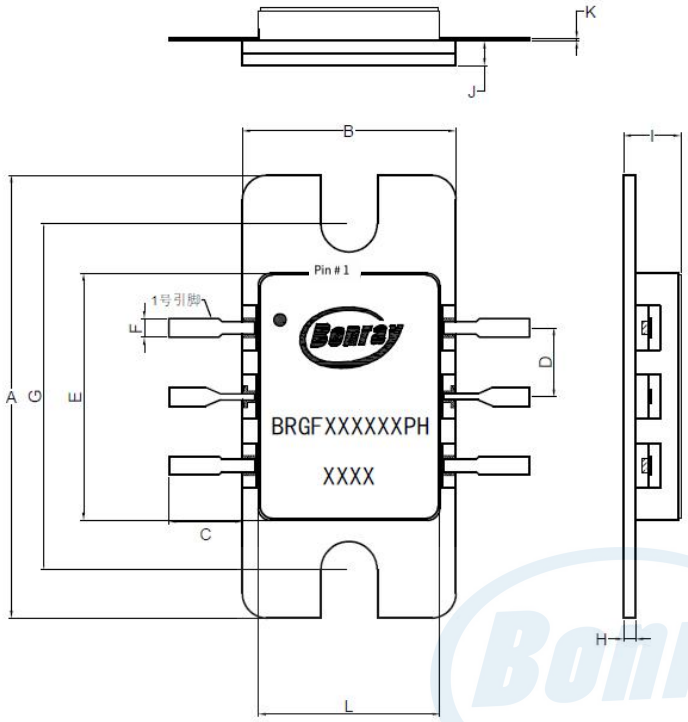
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V with 1.0A current limit
3. Turn on the gate voltage;
4. Turn on drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 70mA
6. Input RF signal

Power-off Sequence

1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -5V
3. Turn off the drain Supply Voltage voltage
4. Turn off the gate Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



尺寸项	单位：mm		
	最小	中值	最大
A	17.83	18.03	18.23
B	8.55	8.7	8.85
C	2.5	3	3.5
D	2.67	2.8	2.93
E	9.9	10.05	10.2
F	0.63	0.76	0.9
G	13.88	14.08	14.28
H	0.37	0.5	0.63
I	2.25	2.4	2.55
J	0.8	1	1.2
K	0.07	0.1	0.13
L	7.25	7.4	7.55

Recommended Soldering Temperature Profile