Product Features

Frequency: 1.6GHz ~ 1.65GHz

Gain : 20.4 dB@1.63GHz

Psat: 44.5dBm@1.63GHz

PAE: 74.3%@1.63GHz

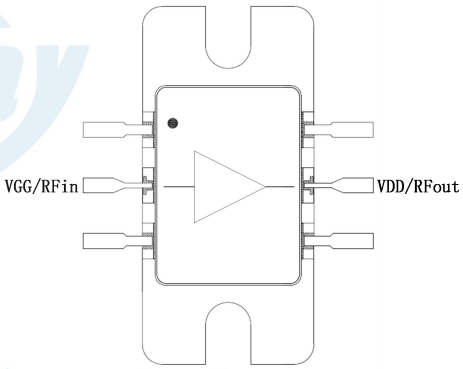
Operation Voltage:28V, I_{DQ} 100mA

Package: PH (metal package)

General Description

The BRGF016030PHG is an internally matched power amplifier designed using the GaN HEMT process with 28V Supply. This product is designed for the Application of satellite communication, Which operating from 1.6GHz to 1.65GHz, with extremely high power PAE, Thanks to the internal matching design, users can use only a small number of periphery components in the system.The product adopts metal ceramic shell package, which has good reliability.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF016030PHG	PH	1.6 GHz to 1.65 GHz 30W Power Amplifier

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	5A
Gate Current (I_G)	9mA
Continuous Dissipated Power (P_D)	50W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note:Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V
Drain Static Current (I_{DQ})	100mA
Gate Voltage (V_{GG})	2.4 V
Channel Temperature (T_{CH})	225 ℃
Continuous Dissipated Power CW (P_D)	40W (25 ° C)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	10:1

Test Conditions: DEMO board test, = T_A 25℃, V_{DD} =+28V, I_{DQ} =100mA, Freq=1.62GHz, CW wave, P_{out}=42dBm.

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W

Note: θ_{JC} to measure the thermal resistance to the bottom of the package;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

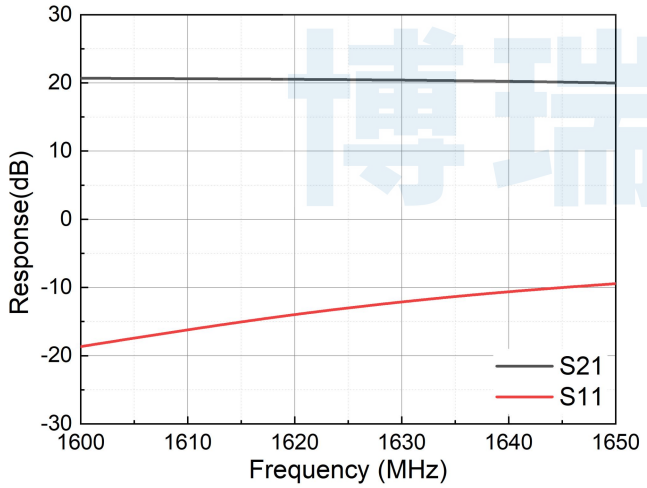
Typical Performance (EVB test data, 1.6GHz ~ 1.65GHz)

Parameters	Typ.						Units
Frequency	**1600**	**1610**	**1620**	**1630**	**1640**	**1650**	**MHz**
Gain	20.69	20.62	20.53	20.41	20.23	19.99	dB
Input Return Loss	-18.66	-16.22	-13.98	-12.13	-10.63	-9.45	dB
Drain Current @P_{sat}	1390	1344	1321	1297	1284	1278	mA
Output Power @P_{sat}	44.61	44.51	44.51	44.45	44.51	44.51	dBm
Power Gain @P_{sat}	16.16	16.06	15.08	14.98	14.94	14.87	dB
PAE@P_{sat}	72.47	73.21	74.00	74.28	76.05	76.37	%

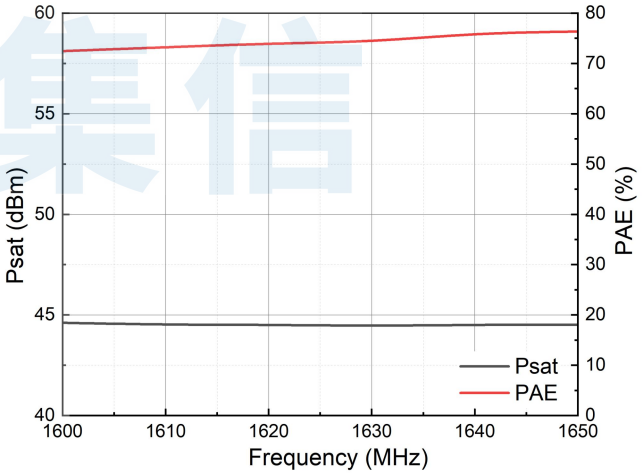
Test Conditions: Temp =+25℃,V_{DD} =+28V, I_{DQ}=100mA, CW test;

Note: P_{sat} defined as the saturation power output of the evaluation board.

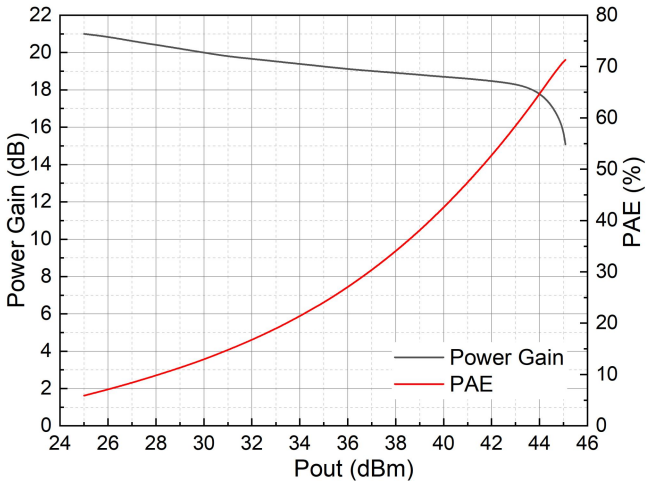
Typical Performance (EVB:1.6GHz~1.65GHz, Temp=+25℃, V_{DD}=+28V, I_{DQ}=100mA, CW wave test)



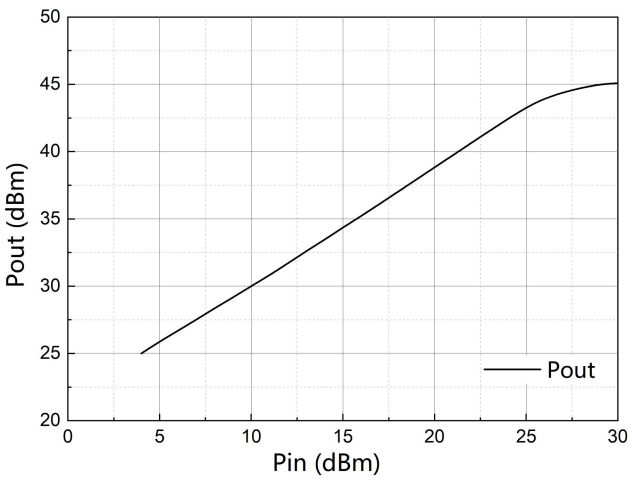
Gain & Input Return Loss vs. Freq



Psat & PEA vs. Freq

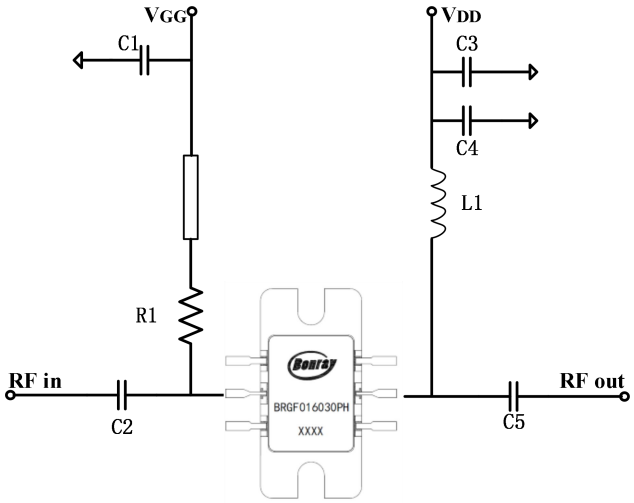


Gain & PEA vs. P_{out} @1.62GHz

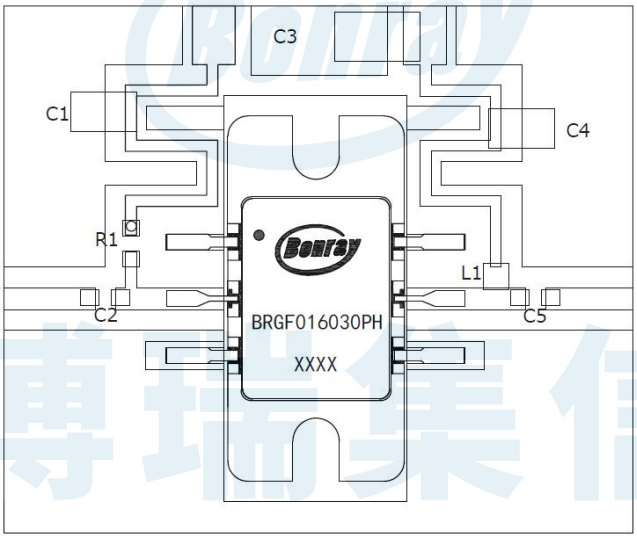


P_{out} and P_{in} vs. Freq @1.62GHz

Typical Application Schematic



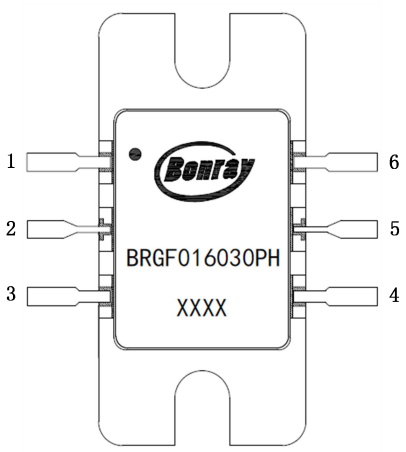
PCB Evaluation Board



Bill of Material

Designator	Package	Description	Part Number
C1,C4	1206	0.1 uF	GRM31C5C2A104JA01#
R1	0603	10ohm	RC0603FR-0710RL
C2	0603	15pF	GQM1875C2E150FB12#
C5	0805	68pF	VJ0805D680JXCQJHT
C3	1210	10uF	GRM32EC72A106KE05#
L1	1111	43nH	1111SQ-43NGEB

Pin Configuration and Description



Pin Number	Pin Name	Description
2	VGG/RFin	Gate voltage / RF Input matched to 50 ohms;
5	VDD/RFout	Drain voltage / RF Output matched to 50 ohms;
1,3,4,6	NC	No connection;
-	Package Base	Source connected to ground;

Power-on Sequence

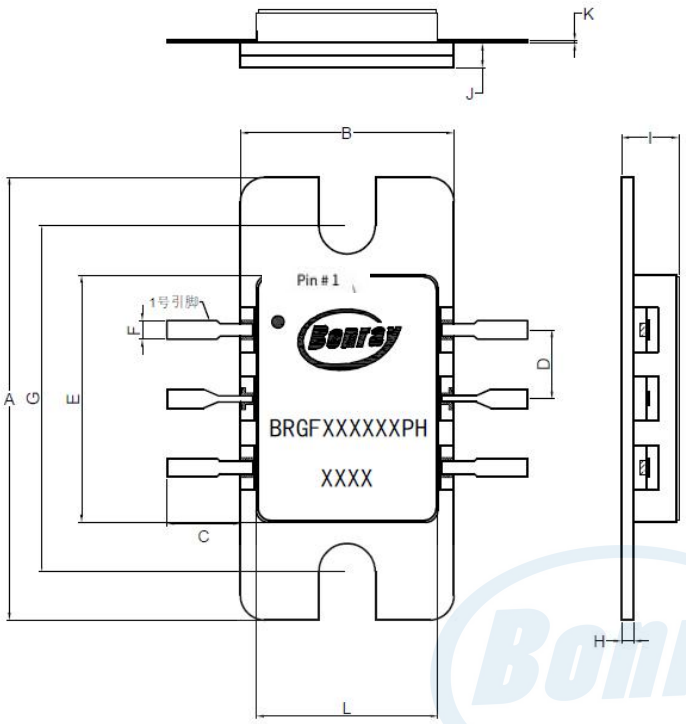
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 2A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 100mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



尺寸项	单位：mm		
	最小	中值	最大
A	17.83	18.03	18.23
B	8.55	8.7	8.85
C	2.5	3	3.5
D	2.67	2.8	2.93
E	9.9	10.05	10.2
F	0.63	0.76	0.9
G	13.88	14.08	14.28
H	0.37	0.5	0.63
I	2.25	2.4	2.55
J	0.8	1	1.2
K	0.07	0.1	0.13
L	7.25	7.4	7.55

Recommended Soldering Temperature Profile