Product Features

Frequency: 30MHz ~ 2.7GHz

Gain : 17.2dB@1GHz

Psat: 40.3dBm@1GHz

PAE: 45.9%@1GHz

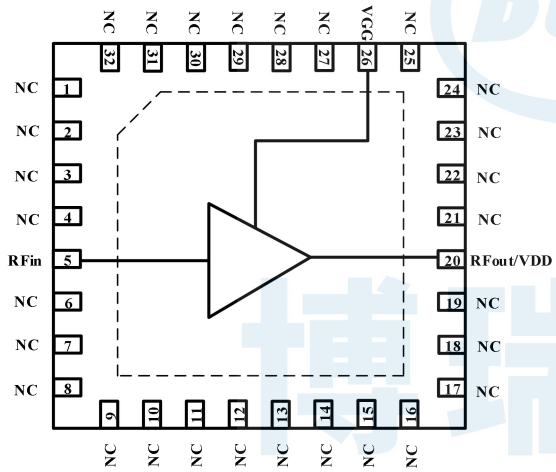
Operation Voltage: 28V, I_{DQ} 100mA

Package: QFN32 (5mm×5mm)

General Description

The BRGF027010FLJ is an internally matched power amplifier designed using the GaN HEMT process to achieves 10W (40dBm) output in the 30MHz to 2.7GHz with a power efficiency of 45.9%@1GHz, Suitable for pulse wave and continuous wave applications such as radar, public mobile radio communications and general-purpose amplification technologies.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF027010FLJ	QFN32	30MHz to 2.7GHz 10W PA

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	1.5 A
Gate Current (I_G)	5mA
Continuous Dissipated Power (P_D)	25W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	100mA (Typ)
Gate Voltage (V_{GG})	-2.51V (Typ)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ to +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: EVB test, TA=25℃, VDD=+28V, IDQ=100mA, Freq=1GHz, CW wave, Pout=36dBm

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal Resistance (θ_{JB})	DC at 85 ° C case	9.9	℃/W
Channel Temperature (Tch)		225	℃

Note: θ_{JB} is the thermal resistance measured from the GaN core to the back of the PCB.

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

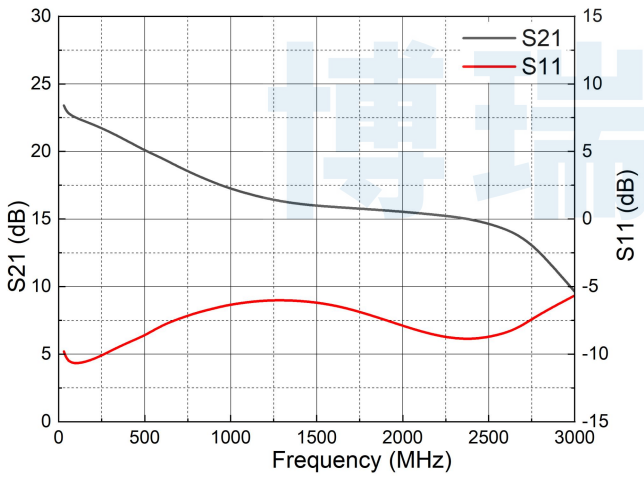
Typical Performanc (EVB test data 30MHz ~ 2.7GHz)

Parameters	Typ.									Units
Frequency	30	100	200	400	600	1000	1400	2000	2700	MHz
Gain	23.4	22.5	22.0	20.8	19.5	17.2	16.1	15.5	13.6	dB
Input Return Loss	-9.8	-10.7	-10.4	-9.2	-7.9	-6.3	-6.0	-7.9	-7.8	dB
Output Return Loss	-11.7	-10.5	-10.3	-10.5	-10.4	-9.6	-8.9	-11.3	-6.8	dB
Drain Current @P_{sat}	461	483	506	574	627	791	965	1030	715	mA
Output Power @P_{sat}	39.3	39.5	39.8	40.0	40.0	40.3	40.9	41.5	40.1	dBm
PAE@P_{sat}	64.8	65.6	65.9	60.5	55.4	45.9	42.2	45.3	46.4	%
Power Gain @P_{sat}	16.5	18.4	16.7	16.1	15.3	12.7	11.1	10.8	10.4	dB

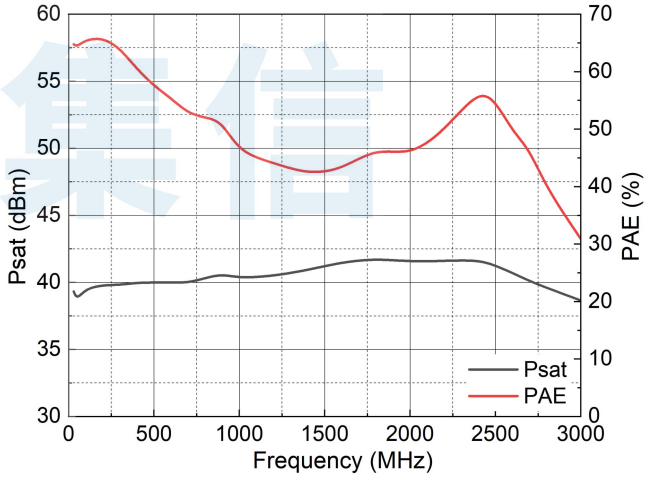
Test Condition: Temp =+25 ° C, V_{DD}=+28V, I_{DQ}=100mA

Note: P_{sat} defined as the saturation power output of the evaluation board;

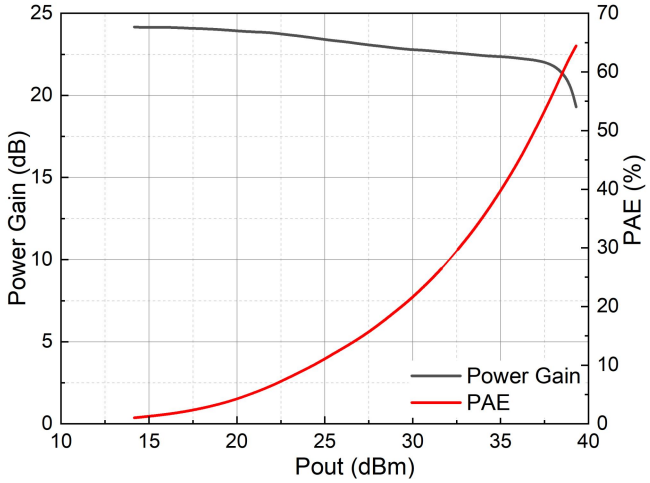
Typical Performanc (EVB test results)



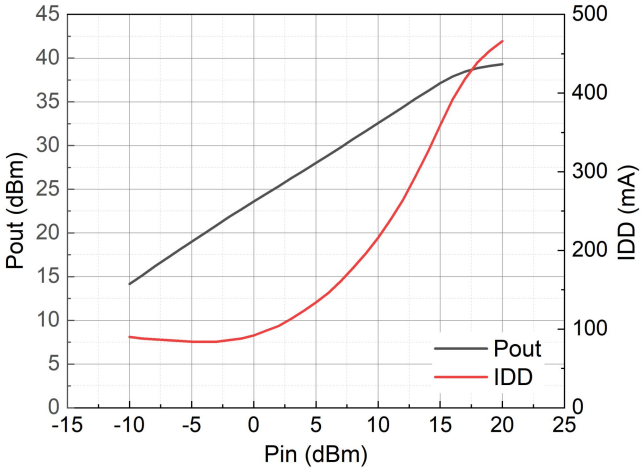
Gain, Input Return Loss vs. Freq



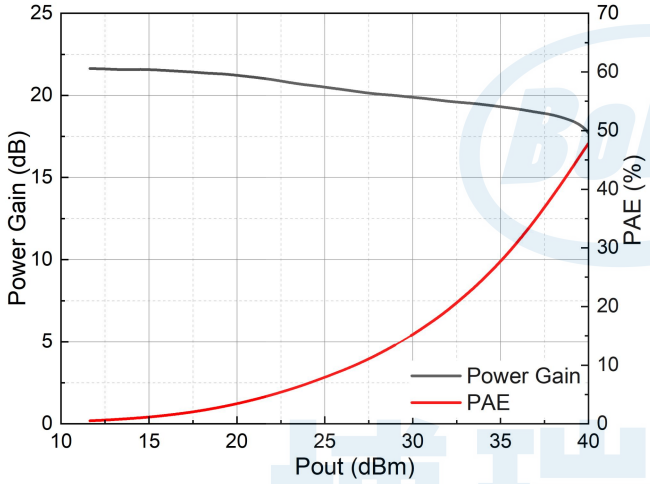
Psat, PAE vs. Freq



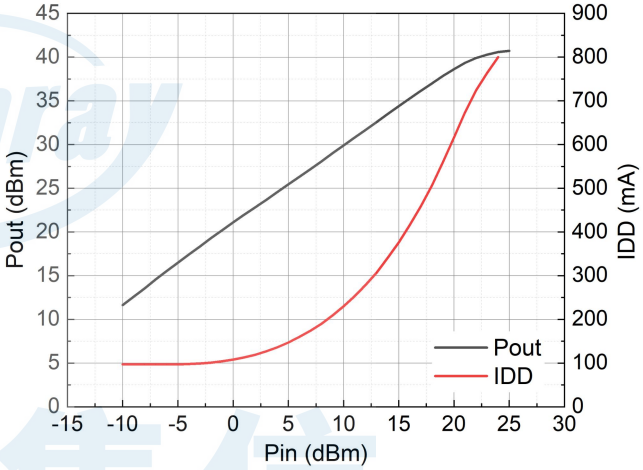
Gain, PAE vs. P_{out} @30MHz



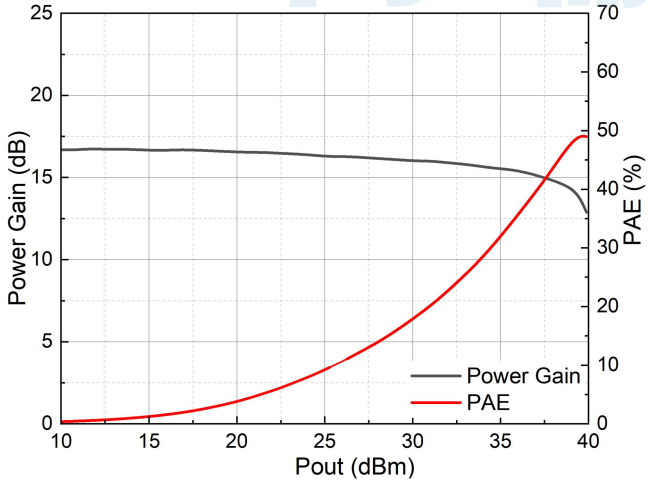
P_{out}, IDD vs. P_{in}@30MHz



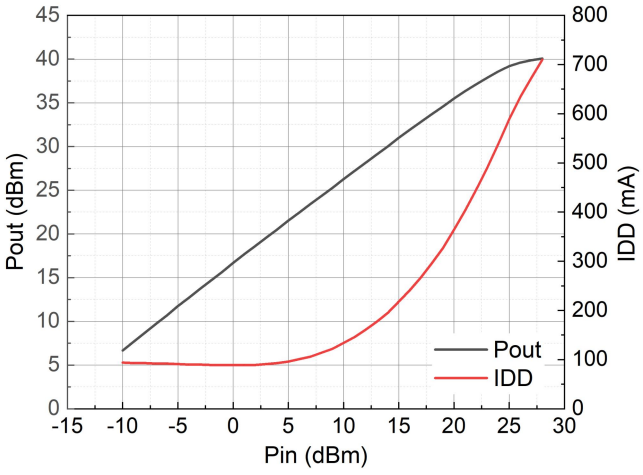
Gain, PAE vs. Pout @1GHz



P_{out}, IDD vs. P_{in} @1GHz

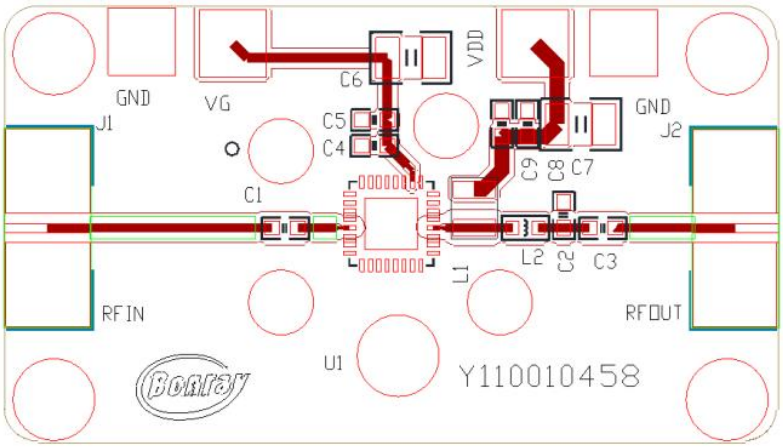


Gain, PAE vs. P_{out} @2.7GHz

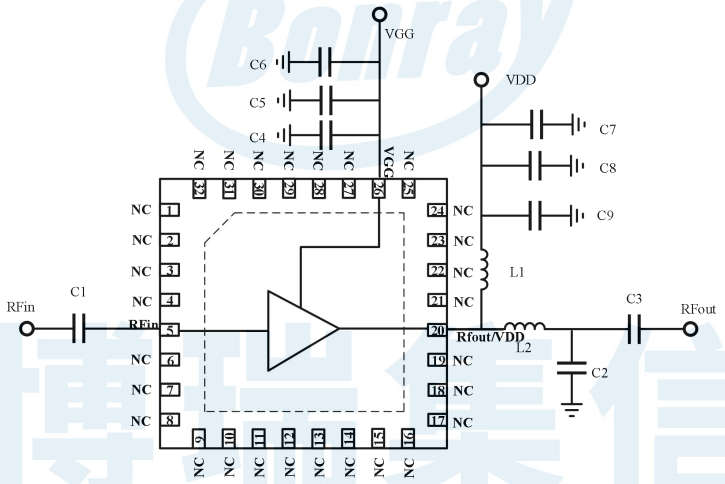


P_{out}, IDD vs.P_{in} @2.7GHz

PCB Evaluation Board



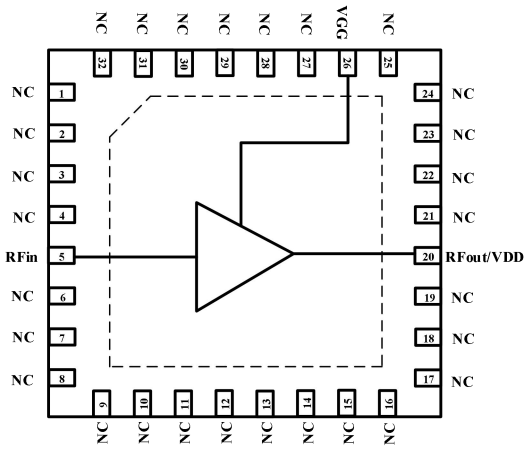
Typical Application Schematic



Bill of Material

Designator	Description	Part Number
U1	Match power amplifier inside 10W	BRGF027010FLJ
L1	1.1 uH	1008AF-112XJRB
C6, C7	10uH	GRM32ER71H106KA12L
C5, C8	100nF	GRM155R71H104KE14D
C4, C9	1nF	GRM188R71H102KA93D
C1, C3	2.2 the nF	GRM1885C1H222JA01D
L2	0.7 nH	MLG1005S0N7BT000
C2	1pF	GQM1875C2E1R0BB12#

Pin Configuration and Description



Pin Number	Pin Name	Description
1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 30, 31, 32	NC	The inside is not connected, and these ports need to be connected to an external RF ground or DC ground when testing to achieve RF isolation and good heat dissipation.
5	RFin	RF input pins.
20	RFout/VDD	RF output and drain supply pins.
26	VGG	Gate supply pins.
-	EP	Exposed pads must be connected to RF ground and DC ground.

Power-on Sequence

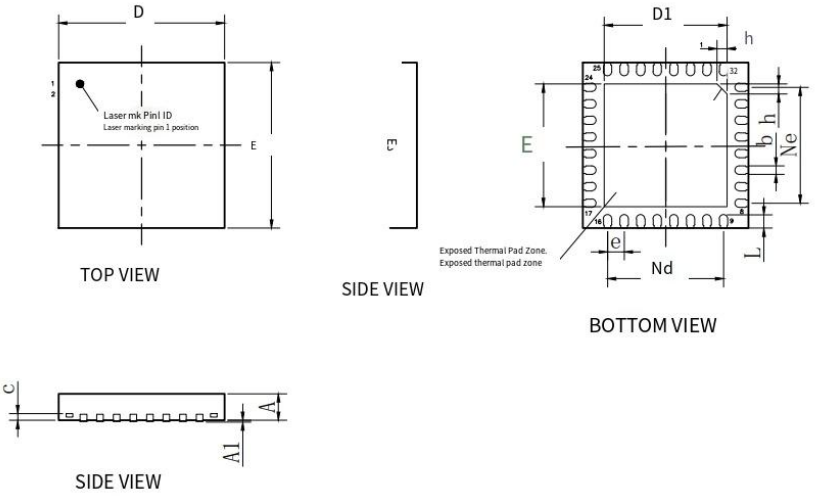
1. Set the gate voltage (V_{GG}) to -5V
2. Set the drain voltage (V_{DD}) to +28V with a current limit of 1300mA
3. Turn on the gate voltage
4. Turn on drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 100mA
6. Input RF signal

Power-off sequence

1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -5V
3. Turn off the drain Supply Voltage voltage
4. Turn off the gate Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.01	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	4.90	5.00	5.10
D1	3.35	3.40	3.45
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E1	3.35	3.40	3.45
L	0.35	0.40	0.45
h	0.25	0.30	0.35

Recommended Soldering Temperature Profiles