Product Features

Frequency: 30MHz ~ 2.7GHz

Gain: 18.4dB@1GHz

Psat: 40.7dBm@1GHz

PAE: 54.5%@1GHz

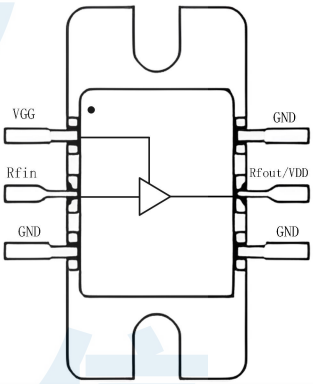
Operation Voltage: 28V, I_{DQ} 100mA

Package: PH (metal package)

General Description

BRGF027010PHG is an internally matched power amplifier designed using the GaN HEMT process with 28V Supply , the product covers the frequency range of 0.03GHz ~ 2.7GHz, quiescent current 100mA. with High power addition efficiency. Thanks to the internal matching design, users can use only a small number of periphery components in the system. The product adopts metal ceramic shell packaging, with good reliability.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF027010PHG	PH	30MHz to 2.7GHz 10W Internal Power Amplifier

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	1.4 A
Gate Current (I_G)	5mA
Continuous Dissipated Power (P_D)	23.8 W.
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	100mA (Typ)
Gate Voltage (V_{GG})	-2.5V (Typ)
Channel Temperature (T_{CH})	225 ° C (Max)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: EVB test, T_A=25℃, V_{DD}=+28V, I_{DQ}=100mA, Freq=2GHz, CW wave, P_{out}=10W test.

Thermal Parameters

Parameters	Test Condition	Value	Units
Thermal Resistance (θ_{JC})	DC at 85 ° C case	10.8	℃/W
Channel Temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the tube housing.

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

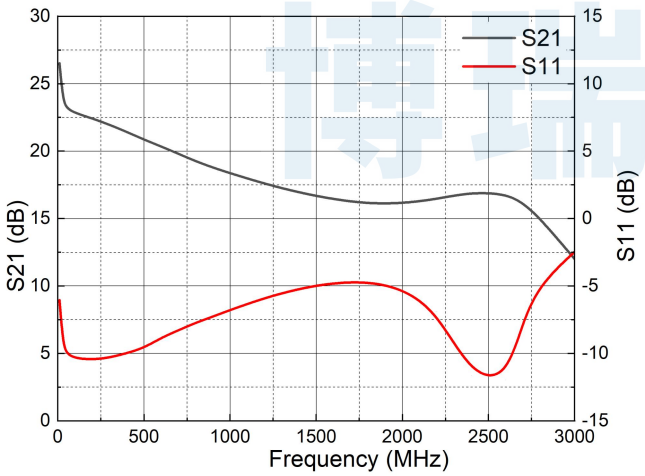
Typical Performance (EVB test data 30MHz ~ 2.7GHz)

Parameters	Typ.									Units
Frequency	30	100	200	400	600	1000	1400	2000	2700	MHz
Gain	23.83	22.83	22.43	21.42	20.34	18.36	16.93	16.12	16.16	dB
Input Return Loss	-6.05	-10.35	-10.46	-9.99	-8.85	-6.78	-5.20	-5.18	-7.59	dB
Output Return Loss	-11.66	-10.39	-10.45	-11.27	-12.24	-12.87	-13.01	-12.86	-15.07	dB
Drain Current @P_{sat}	0.457	0.474	0.495	0.567	0.642	0.732	0.987	1.035	0.837	A
Output Power @P_{sat}	39.30	39.45	39.68	39.90	40.05	40.65	41.70	41.73	41.71	dBm
PAE@P_{sat}	65.08	65.21	65.58	60.00	54.65	54.49	49.28	46.30	58.99	%
Power Gain @P_{sat}	16.65	17.53	16.66	15.98	15.39	14.16	11.01	10.04	11.71	dB

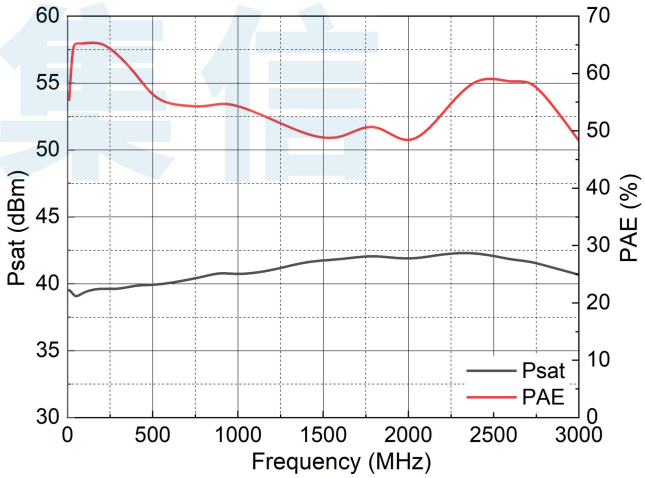
Test Conditions: Temp =+25℃, V_{DD}=+28V, I_{DQ}=100mA, CW test;

Note: P_{sat} defined as the saturation power output by the evaluation board.

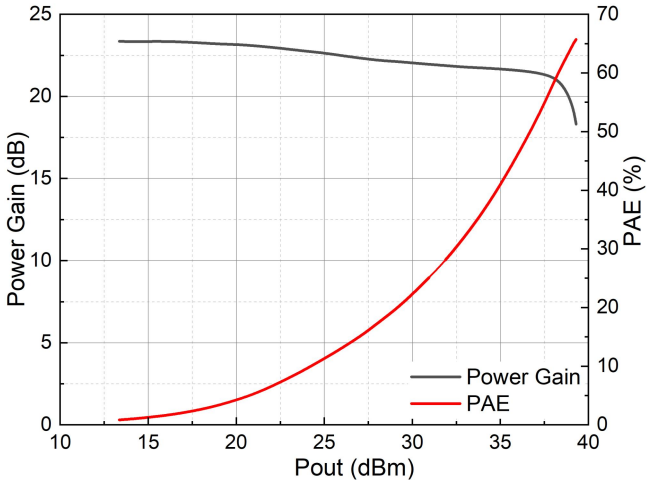
Typical Performance (EVB test results)



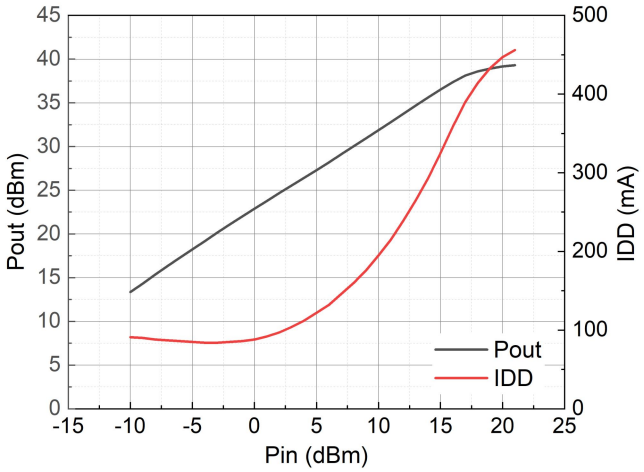
Gain , Input Return Loss vs. Freq



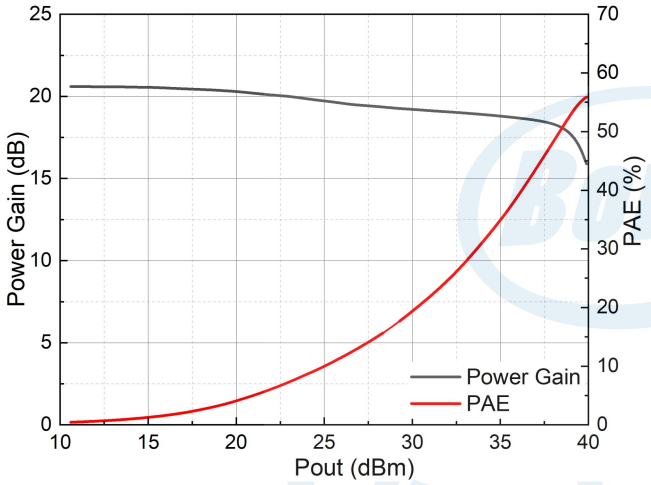
Psat, PAE vs. Freq



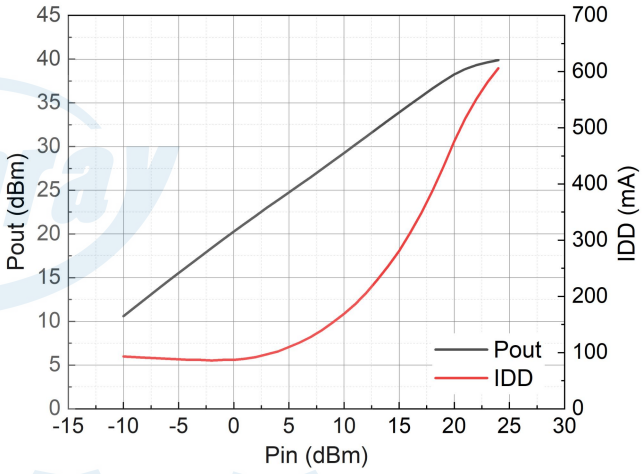
Gain , PAE vs. P_{out} @30MHz



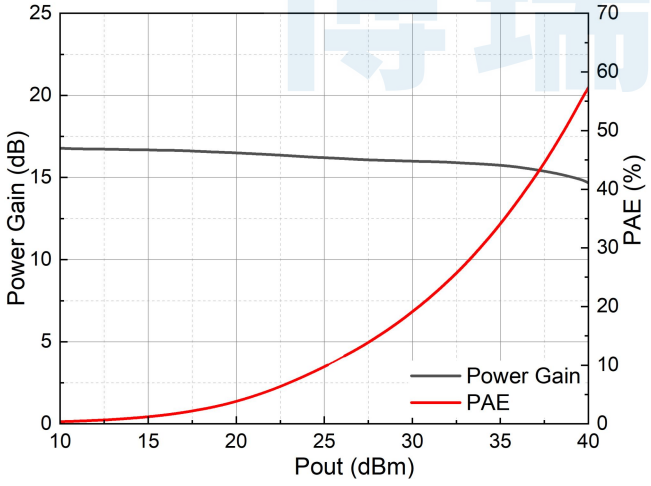
P_{out}, IDD vs. P_{in} @30MHz



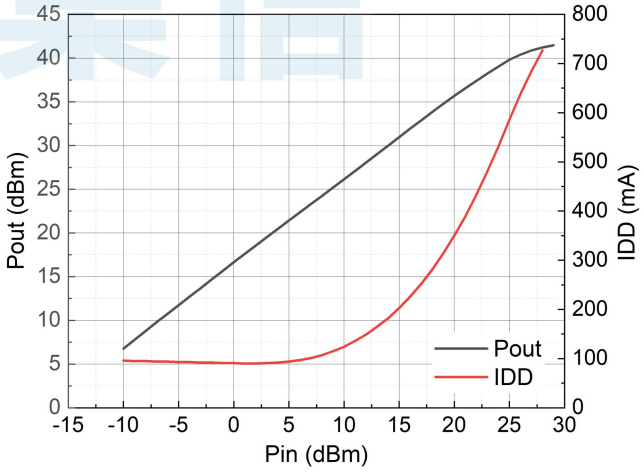
Gain , PAE vs. P_{out}@ 500MHz



P_{out}, IDD vs. P_{in} @ 500MHz

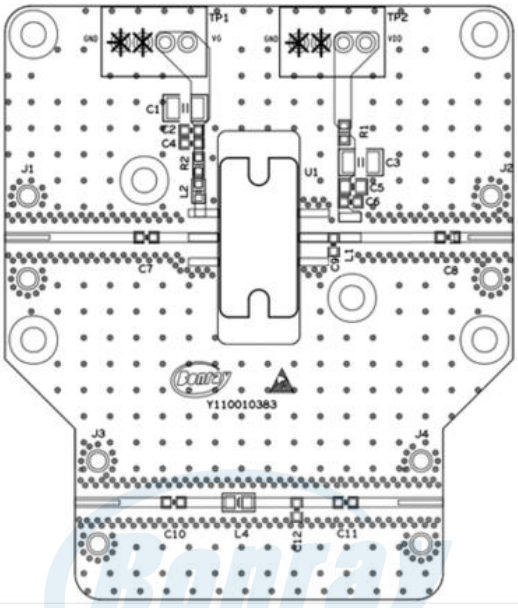


Gain , PAE vs. P_{out} @2.7GHz

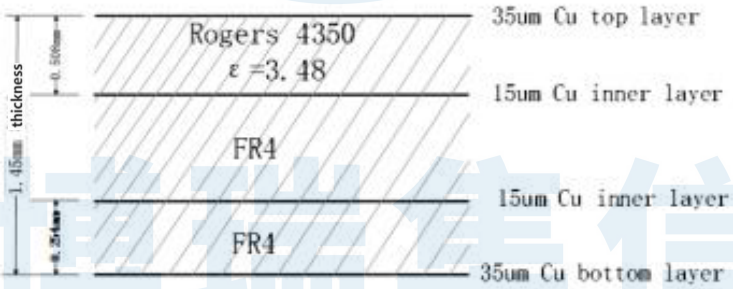


P_{out}, IDD vs. P_{in} @2.7GHz

PCB Evaluation Board

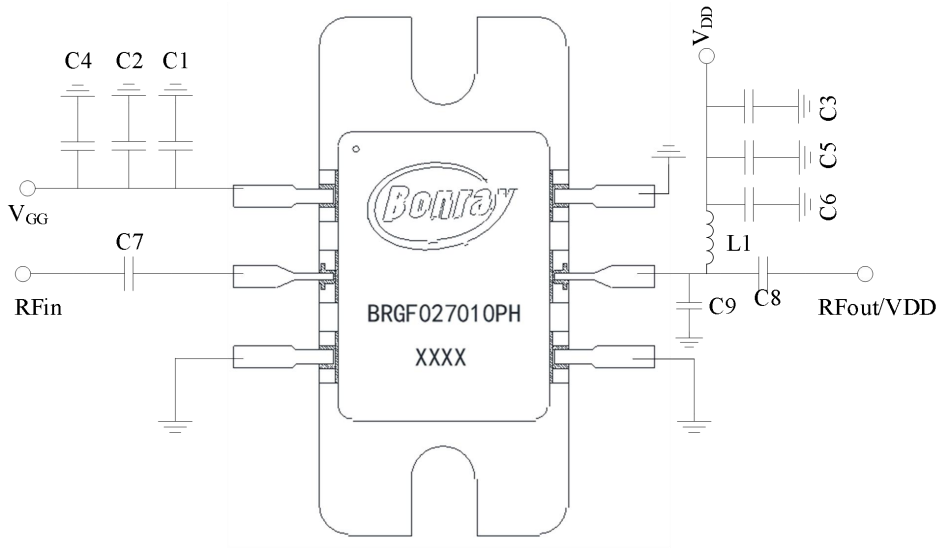


PCB



50 ohms Impedance Signal Lines：width=1.1mm, spacing=1.1mm

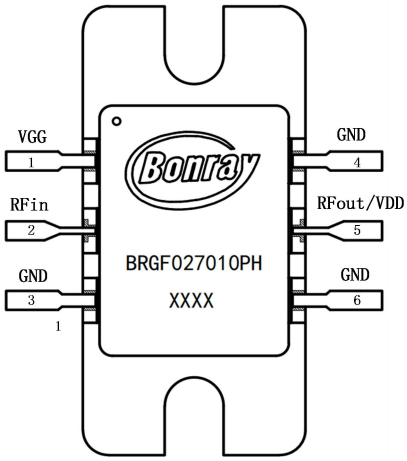
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
C1,C3	1210	10uF	GRM32ER71H106KA12L
C2,C5	0402	100nF	GRM155R71H104KE14D
C4,C6	0603	1nF	GRM188R71H102KA93D
C7,C8	0603	2.2 the nF	GRM1885C1H222JA01D
C9	0603	1pF	GQM1875C2E1R0BB12#
L1	1008	1.1 uH	1008AF-112XJRB

Pin Configuration and Description



Part Numver	Pin Name	Description
1	VGG	Gate voltage
2	RFin	RF Input matched to 50 ohms;
3.6	GND	RF&DC ground
5	RFout/VDD	Drain voltage / RF Output matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

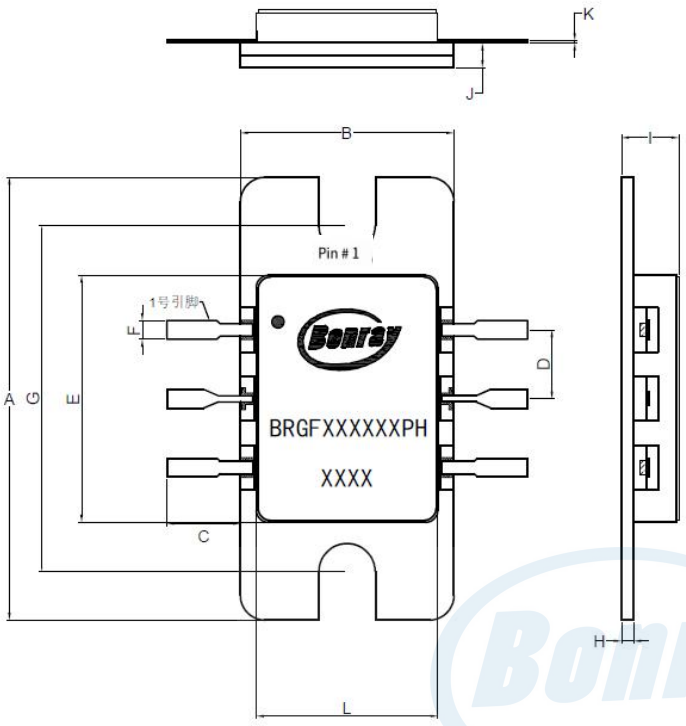
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 1.2A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage(V_{GG}) so that the drain current is 100mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal.
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



尺寸项	单位：mm		
	最小	中值	最大
A	17.83	18.03	18.23
B	8.55	8.7	8.85
C	2.5	3	3.5
D	2.67	2.8	2.93
E	9.9	10.05	10.2
F	0.63	0.76	0.9
G	13.88	14.08	14.28
H	0.37	0.5	0.63
I	2.25	2.4	2.55
J	0.8	1	1.2
K	0.07	0.1	0.13
L	7.25	7.4	7.55

Recommended Soldering Temperature Profile