Product Features

Frequency: 2.5GHz ~ 4GHz

Gain: 29.8dB@3.7GHz

Psat: 41.9dBm@3.7GHz

PAE: 50.4%@3.7GHz

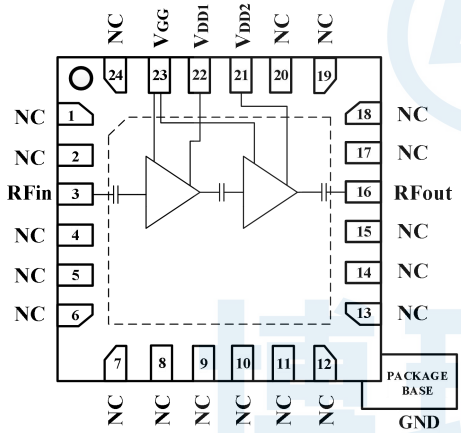
Operation Voltage: 28V, I_{DQ} 130mA

Package: QFN24(5mm×5mm)

General Description

The BRGF035012FWJ is a high-gain GaN internal matched power amplifier that achieves 12W saturated output in the 2.5GHz to 4GHz wide band with high power added efficiency (PAE=50.4%, Pout=42dBm@3.7GHz). In-band gain flatness up to ±0.5dB with a Pin of 21dBm. The product is ideal for pulse wave or carrier applications such as radar, public mobile radio communications and general purpose amplification modules.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF035012FWJ	QFN24	2.5GHz to 4GHz 12W Internal Matched PA

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6～0V
Gate Current (I_G)	4mA
Channel Temperature (T_{CH})	275℃
Mounting Temperature (30 seconds)	245℃
Maximum Input Power	25dBm

Note:Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V（Typ）
Drain Static Current (I_{DQ})	130mA（Typ）
Gate Voltage (V_{GG})	-2.81V（Typ）
Storage Temperature	-65℃～+150℃
Operating Temperature	-55℃～+85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Test Conditions: DEMO board test, T_A =25℃, V_{DD}=+28V, I_{DQ}=130mA, Freq=3.3GHz, CW wave, P_{out}=38dBm.

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	10:1

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

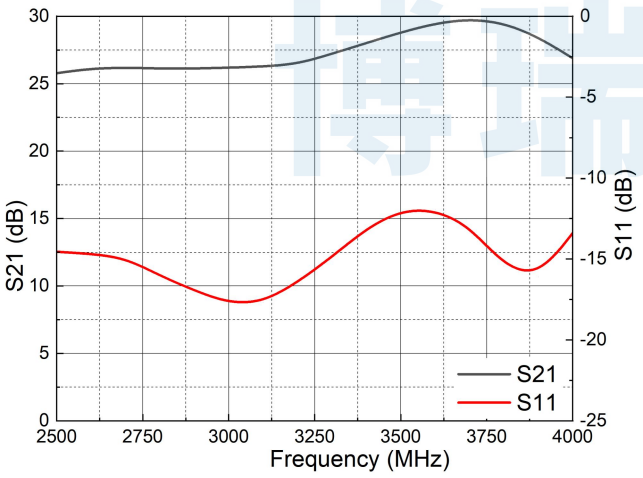
Typical Performance (EVB test data,2.5GHz ~ 4GHz)

Parameters	Typ.									Unit
Frequency	2500	2700	2900	3100	3300	3500	3700	3900	4000	MHz
Gain	25.8	26.2	26.1	26.3	27.2	28.8	29.8	28.5	26.9	dB
Input Return Loss	-14.5	-14.9	-16.9	-17.7	-14.9	-12.0	-13.0	-16.1	-13.4	dB
Output Return Loss	-7.2	-9.0	-10.7	-11.3	-10.5	-8.9	-8.2	-10.4	-12.1	dB
Saturated Pout (dBm)	42.0	41.7	41.4	41.3	42.0	42.1	41.9	41.2	41.2	dBm
PAE@P_{sat}	52.9	52.5	49.6	47.5	48.4	49.8	50.4	53.4	53.7	%

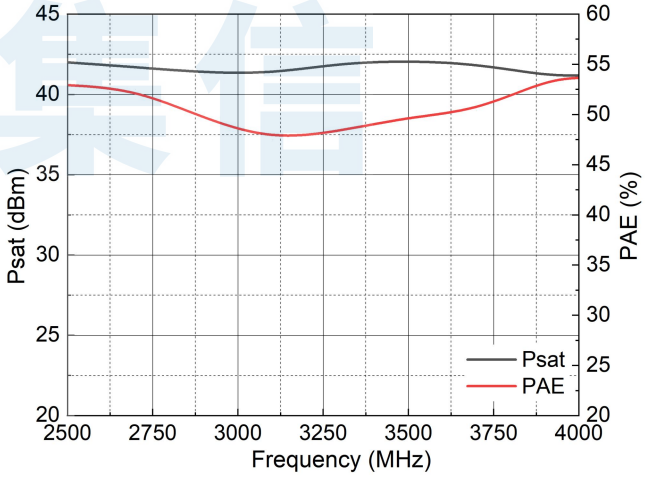
Test Condition: Temp =+25℃, V_{DD}=+28V, I_{DQ}=130mA; Psat&PAEwas pulse test, pulse width was 100us, duty cycle was 10%, I_{DQ} =6mA

Note: P_{sat} defined as the saturation power output of the evaluation board.

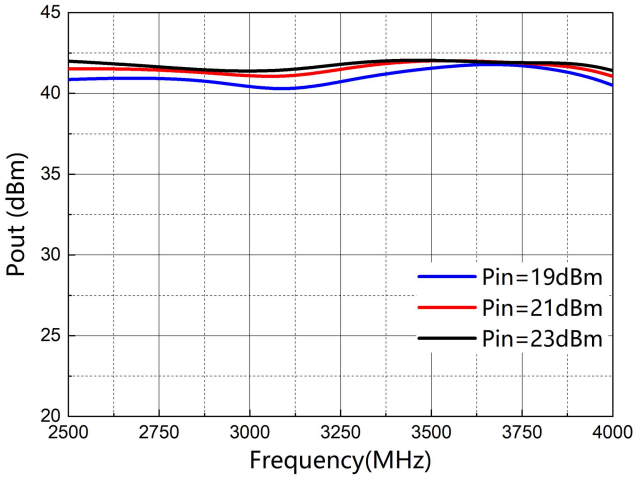
Typical Performance (EVB test results)



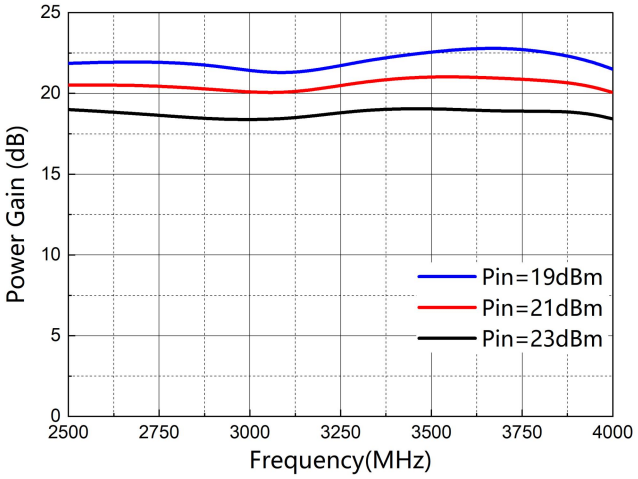
Gain , Input Return Loss vs. Freq



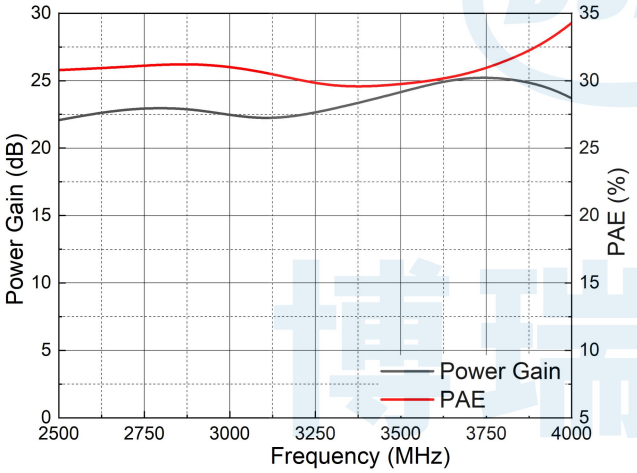
Psat, PAE vs. Freq



P_{out} vs. Freq

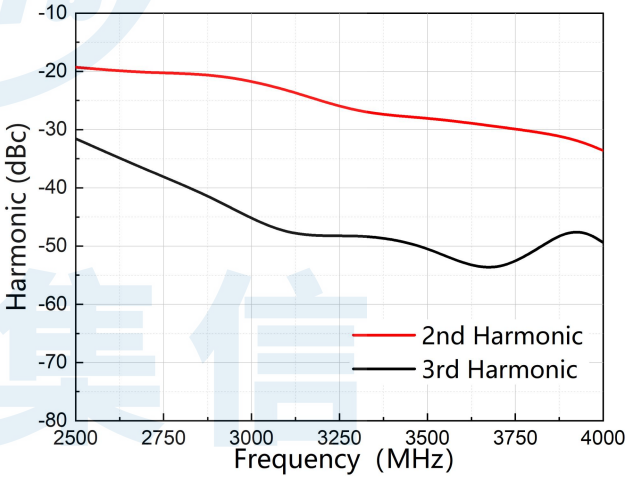


Gain vs. Freq



Gain , PAE vs. Freq

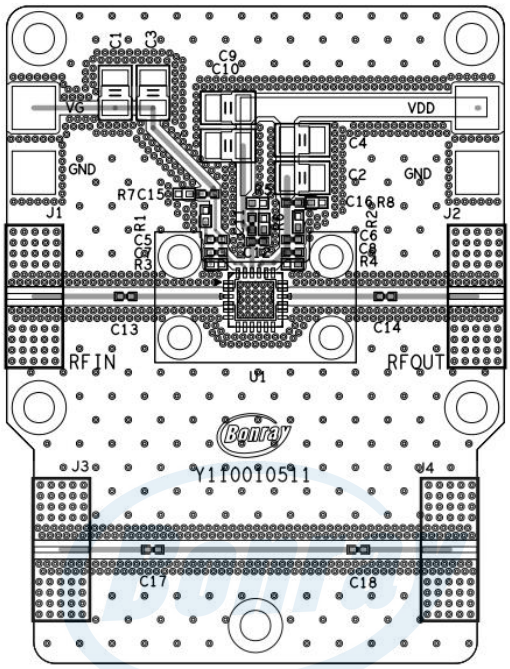
(Pout=36dBm CW wave)

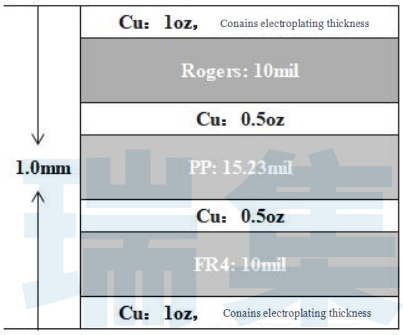


Second/Third Harmonics vs. Freq

(Pout=36dBm CW wave)

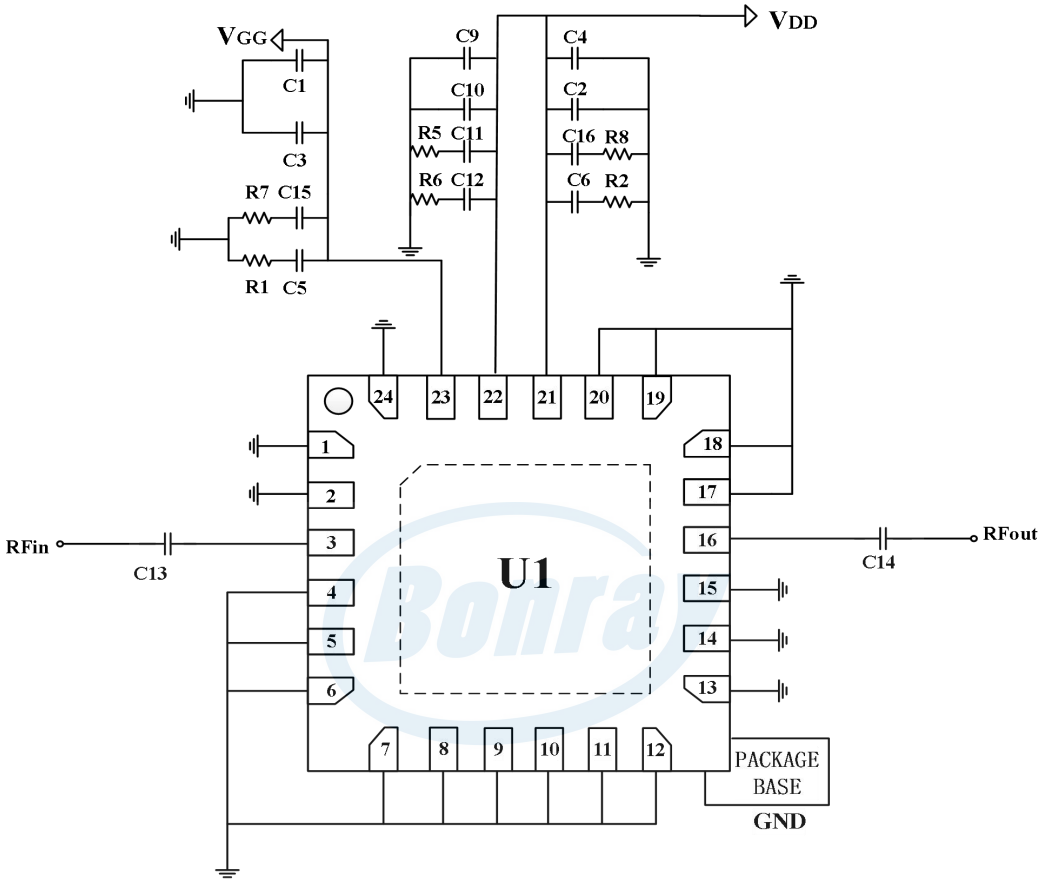
PCB Evaluation Board





Note: The C13 and C14 bit numbers actually use 0 ohm lines for short-circuitry processing, and it is recommended to replace the corresponding device with microstrip lines in PCB design.

Typical Application Schematic

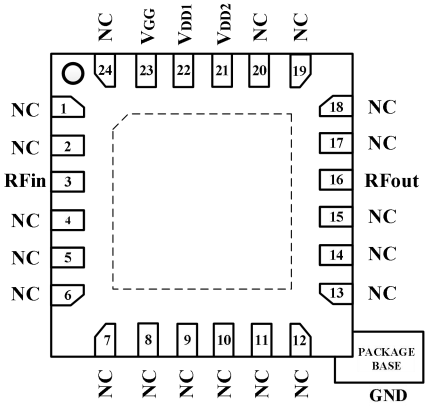


Bill of Material

Designator	Description	Part Number
U1	2.5GHz~4GHz 12W matched power amplifier	BRGF035012FWJ
R1,R7	560 Ω	RC0402JR-07560RL
R2,R8,R5,R6	10 Ω	RC0402JR-0710RL
C5,C12,C6	1000pF	C0402C102J1GACACAUTO
C11,C15,C16	100nF	GRM155R71H104KE14D
C1,C2,C3,C4,C9,C10	10uF	GRM32EC72A106KE05#
C13, C14	0 Ω	/

Note: * indicates that the Designator is not used in the BOM of the corresponding frequency band. It is recommended to replace the corresponding bit number with a microstrip line during PCB design.

Pin Configuration and Description



Pin Number	Pin Name	Description
3	RFin	Rf input, already internally matched to 50Ω;
16	RFout	Rf output, internally matched to 50Ω;
21	V_{DD2}	Secondary core drain Supply Voltage voltage
22	V_{DD1}	Primary core drain Supply Voltage voltage
23	V_{GG}	The gate Supply Voltage voltage of the two-stage core
4-trichlorobenzene 1 ~ 2 ~ 20, 24	NC	The inside is not connected, and these ports need to be connected to an external RF ground or DC ground when testing to achieve RF isolation and good heat dissipation.
-	EP	Exposed pads, must be connected to RF ground and DC ground.

Power-on Sequence

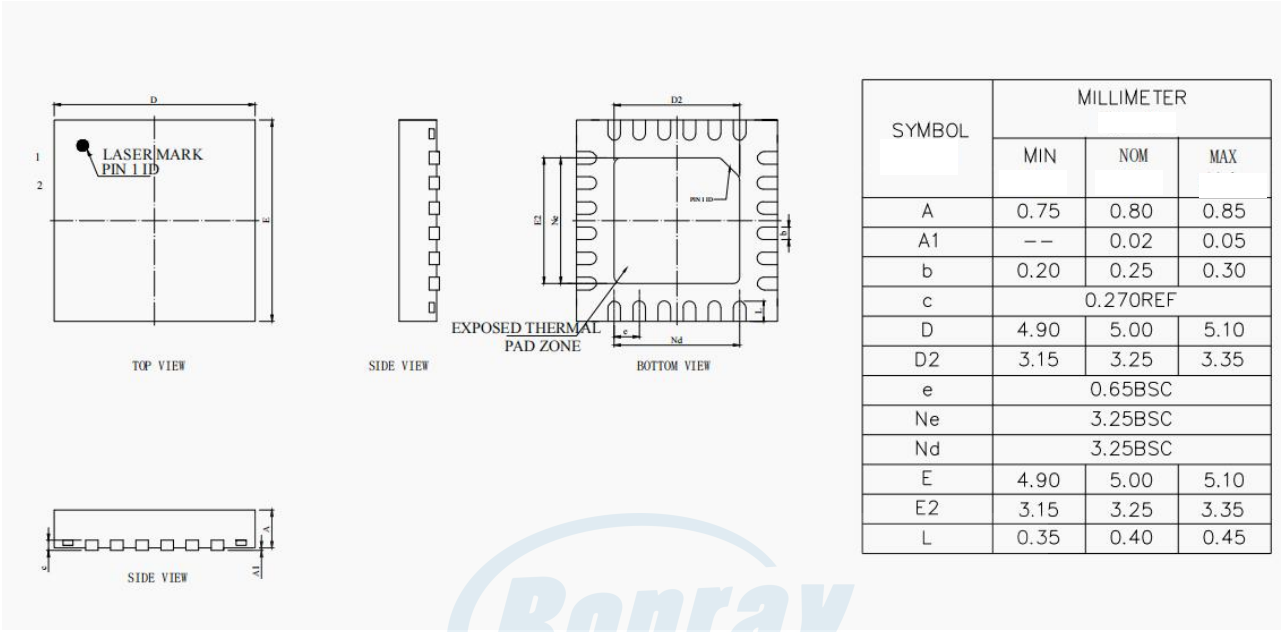
1. Set the gate voltage (V_{GG}) to -5V
2. Set the drain voltage (V_{DD}) to +28V with a current limit of 1300mA
3. Turn on the gate voltage
4. Turn on drain voltage
5. Increase the gate voltage (V_{GG}) so that the drain current is 130mA
6. Input RF signal

Power-off Sequence

1. Turn off the RF signal
2. Reduce the gate voltage (V_{GG}) to -5V
3. Turn off the drain Supply Voltage voltage
4. Turn off the gate Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	--	0.02	0.05
b	0.20	0.25	0.30
c		0.270REF	
D	4.90	5.00	5.10
D2	3.15	3.25	3.35
e		0.65BSC	
Ne		3.25BSC	
Nd		3.25BSC	
E	4.90	5.00	5.10
E2	3.15	3.25	3.35
L	0.35	0.40	0.45

Recommended Soldering Temperature Profile