

Product Features

Frequency: 2GHz ~ 6GHz

Gain: 26.6dB@2GHz

Psat: 40.9dBm@2GHz

PAE: 44.5%@2GHz

Operation Voltage: 28V, I_{DQ} 350mA

Applications

Power Amplification Stage for Wireless

Infrastructure

Test and Measurement Equipment

Commercial and Military Radars

Universal Transmitters and Jammers

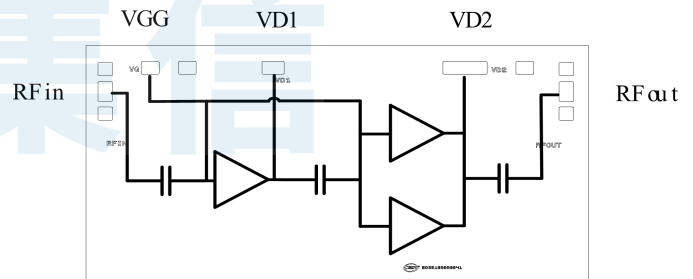
General Description

BRGF060010LD is an ultra-wideband in-match power amplifier fabricated based on GaN process. The product covers the frequency range of 2GHz ~ 6GHz, adopts +28V drain level power supply Supply Voltage, the quiescent current 350mA, the input and output port impedance has been matched to 50Ω, at the same time, only a few external devices can be used in the system design, which greatly reduces the sensitivity of the use of devices, so as to realize the product's high frequency and ultra-wideband application of.

Ordering Information

Part Number	Package	Description
BRGF060010LD	Die	10W MMIC PA

Functional Block Diagram



Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Gate Current (I_G)	8mA
Channel Temperature (T_{CH})	275 °C
Peak Welding Temperature (< 5s)	320 °C
Storage Temperature	-65°C ~ +150°C
Operating Temperature	-55°C ~ +85°C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V
Drain Static Current (I_{DQ})	350mA
Gate Voltage (V_{GG})	2.18 V
Channel Temperature (T_{CH})	225 °C

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

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Power-on Sequence

1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage ($V_{D1}&V_{D2}$) to +28V, current limit 2A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 350mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage

Note: When the circuit is designed, a timing protection circuit is required to power off the V_{GG} at the offset voltage. After the V_{GG} is fully powered on, add $V_{D1}&V_{D2}$. When powering off the V_{GG} , ensure that the $V_{D1}&V_{D2}$ drops below -5V. Especially in T_{DD} applications, gate-supplied decoupling capacitors need to be rigorously evaluated to meet the switching speed requirements.

ESD WARNING

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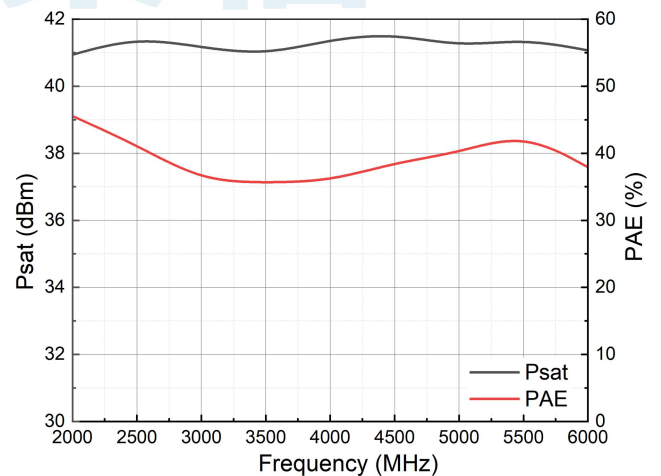
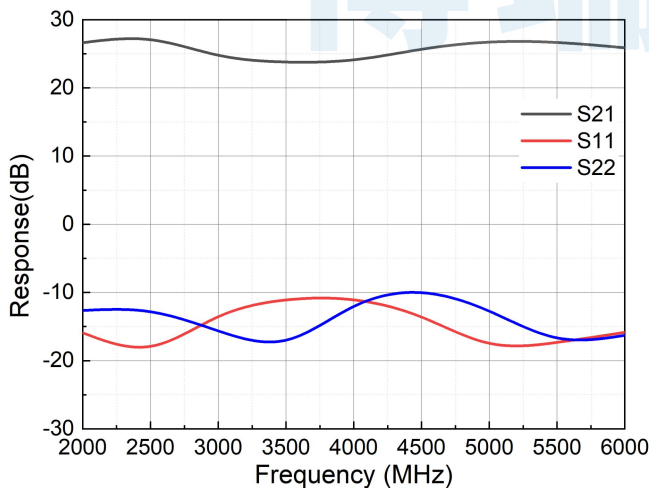
ELECTROSTATIC SENSITIVE DEVICE**OBSERVE HANDLING PRECAUTIONS**

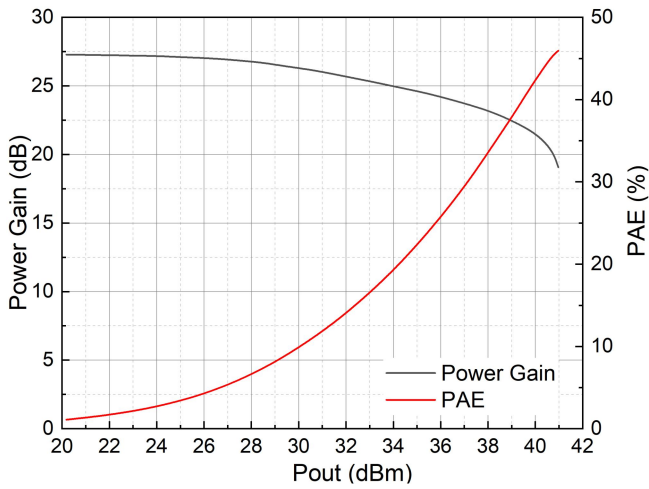
Typical Performance (EVB test data, 2GHz ~ 6GHz)

Parameters	Typ.									Units
	2000	2500	3000	3500	4000	4500	5000	5500	6000	
Frequency	2000	2500	3000	3500	4000	4500	5000	5500	6000	MHz
Gain	26.63	27.07	24.80	23.80	24.12	25.66	26.71	26.65	25.88	dB
Input Return Loss	-15.91	-17.90	-13.57	-11.09	-11.09	-13.60	-17.46	-17.31	-15.85	dB
Output Return Loss	-12.64	-12.83	-15.63	-16.99	-12.05	-10.03	-12.74	-16.66	-16.29	dB
Drain Current @P _{sat}	0.959	1.202	1.258	1.191	1.331	1.309	1.153	1.135	1.189	A
Output Power @P _{sat}	40.94	41.47	41.16	40.93	41.40	41.58	41.17	41.42	41.07	dBm
Power Gain @P _{sat}	18.24	19.67	14.86	13.83	14.90	17.88	19.37	19.42	18.87	dB
PAE@P _{sat}	45.55	41.23	35.87	35.61	35.84	38.62	40.08	43.14	37.93	%

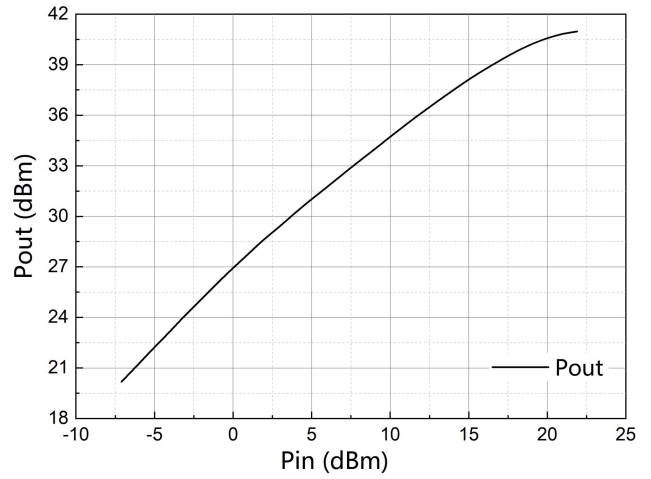
 Test Conditions: Temp =+25°C, V_{DD}=+28V, I_{DQ3}=50mA, CW test;

 Note: P_{sat} defined as the saturation power output by the evaluation board;

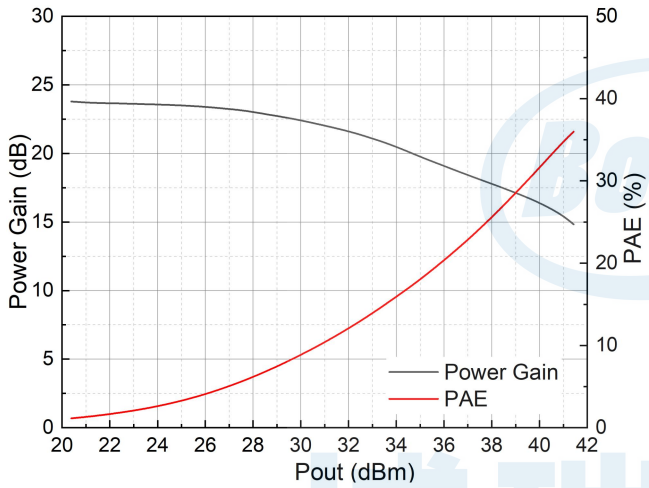
Typical Performance (Evaluation board: 2GHz~6GHz, Temp =+25°C, V_{DD}=+28V, I_{DQ}=350mA, CW wave test)

Gain & Input Return Loss & output Return Loss vs. Freq
Psat & PAE vs. Freq



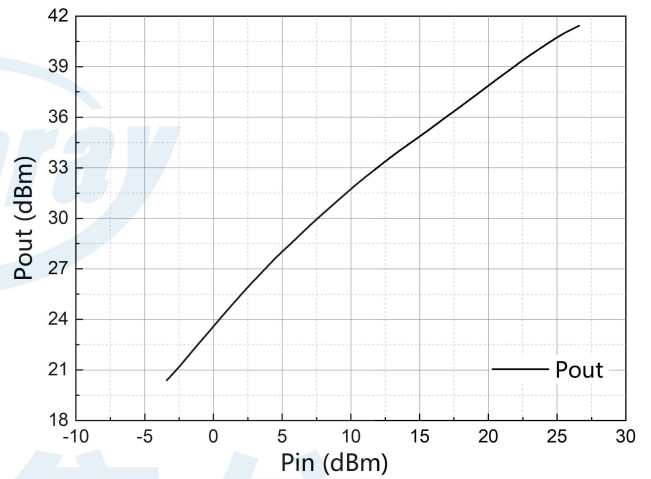
Gain & PAE vs. P_{out} @2GHz



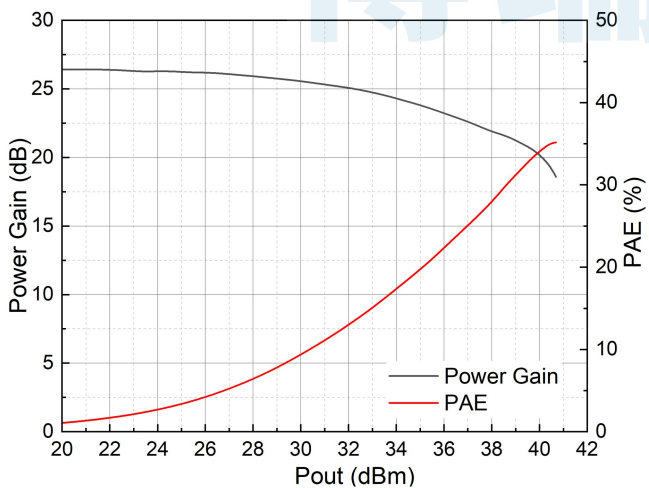
P_{out} vs. P_{in} @2GHz



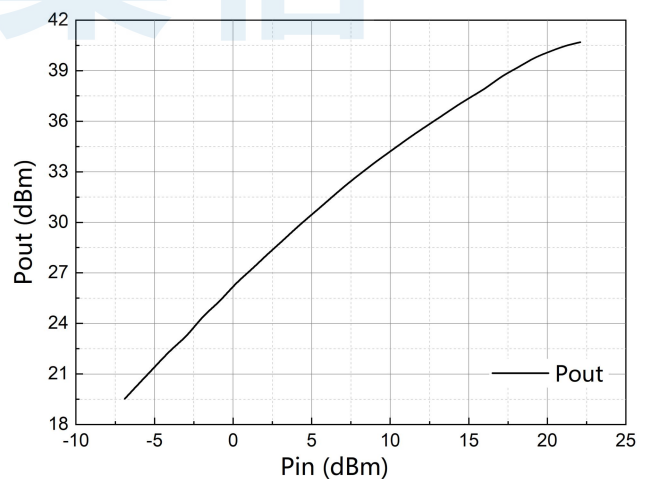
Gain & PAE vs. P_{out} @4GHz



P_{out} vs. P_{in} @4GHz

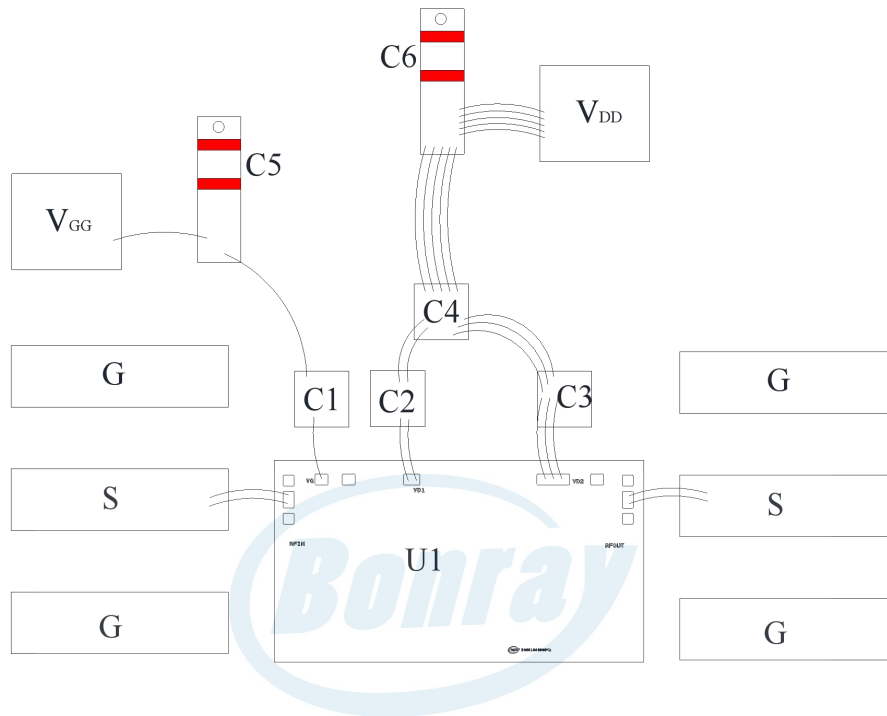


Gain & PAE vs. P_{out} @6GHz



P_{out} vs. P_{in} @6GHz

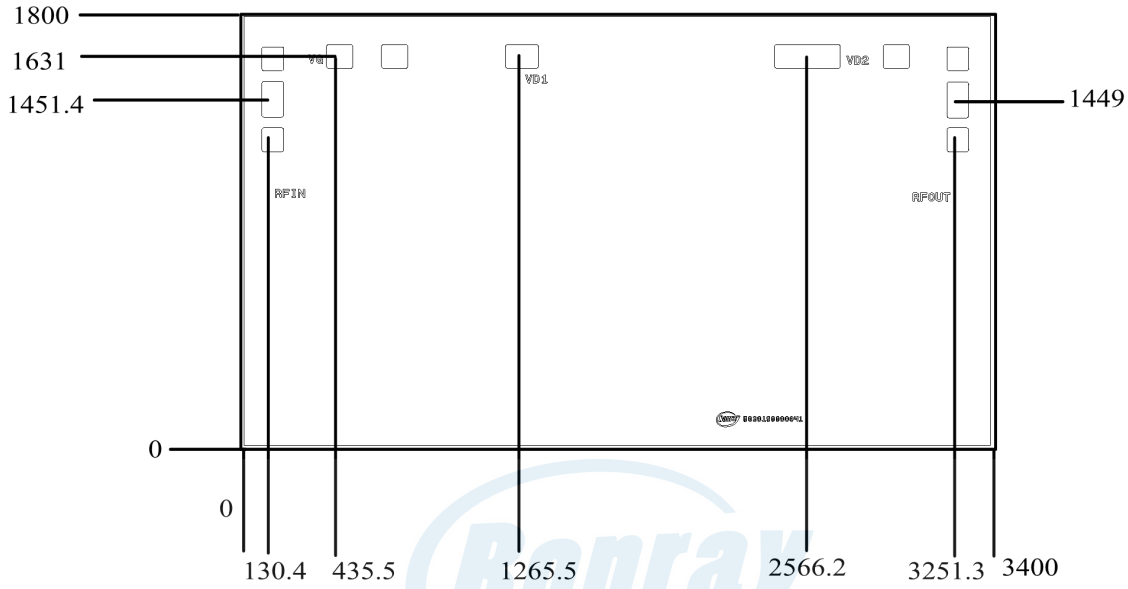
Typical Application Schematic



Bill of Material

Designator	Package	Description	Part Number
U1	die	10W ultra wideband power amplifier	BRGF060010LD
C1, C2, C3, C4	Chip capacitors	1000pF	CT91202X102M100TW
C5, C6	1210 capacitance	10uF	GRM32EC72A106KE05#

Mechanical Information (Units: mm)



Notes:

- 1、 Gold plating on the back of the chip;
- 2、 Chip back ground;
- 3、 Bonding press point gold-plated, press point size: RFin press point: 100um×150um; RFout press point: 100um×150um;
VG pressure point: 120um×100um; VD1 pressure point: 150um×100um; VD2 pressure point: 300um×100um;
- 4、 Can not be bonded on the through hole;
- 5、 Overall dimension tolerance: ±30um.

Bonding Pressure Point Definition

Press Point Number	Function Symbol	Function Description
1	RFin	RF Input matched to 50 ohms;
2	RFout	RF Output matched to 50 ohms;
3	VGG	Gate voltage
4	VD1	External DC first stage drain offset Supply Voltage.
5	VD2	External DC second stage drain offset Supply Voltage.
6	GND	The back of the chip is grounded, and this pin and package substrate must be connected to the RF/DC ground.

Handling Precautions:

1. Storage: The chip must be placed in a container with electrostatic protection function, and stored in a nitrogen environment.
2. Cleaning treatment: The bare chip must be operated and used in a clean environment. It is forbidden to use liquid cleaning agent to clean the chip.
3. ESD prevention: Strictly comply with the requirements of ESD prevention to avoid electrostatic damage.
4. Routine operation: Use vacuum pen or precision pointed tweezers to pick up the chip. Avoid touching the chip surface with tools or fingers during operation.
5. Power-on sequence: The operation must follow the recommended power-on sequence.
6. Installation operation: The chip installation needs to use AuSn solder eutectic sintering process, the mounting surface must be clean and flat, and the chip is connected to the input and output radio frequency
The gap between the cable base plate should be as small as possible.
7. Sintering process: with 80/20AuSn sintering, it is recommended that the peak temperature of sintering is 300°C, and the sintering duration is about 5 seconds.
8. Bonding operation: no special instructions, recommended 25μm gold wire wedge welding process, thermoultrasonic bonding temperature recommended 150°C.
9. Please contact customer service if you have any questions.