Product Features

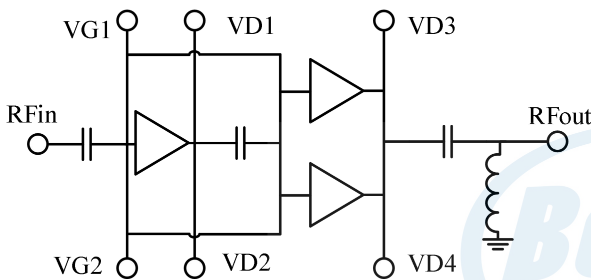
Frequency: 2GHz ~ 6GHz

Gain: 23.0dB@4GHz

Psat: 44.7dBm@4GHz

PAE: 32.1%@4GHz

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGF060020LD	die	2GHz to 6GHz 20W Internal Matched PA

General Description

BRGF060020LD is a GaN process based on the design of internal matching ultra wideband power amplifier, with +28V power supply, the input and output have been matched to 50 ohms, and the RF input and output ports have built-in DC block, the output port has ground inductance. The product is a two-stage common source structure, which improves the gain of the full frequency band of the product. In the 2GHz ~ 6GHz broadband, it can provide a high gain of 23.0dB and a saturated output power of 44.7dBm. The product adopts on-chip through hole metallization process to ensure good grounding, no additional grounding measures are required, and the use is simple and convenient. The back of the chip is metallized, and the eutectic sintering process must be used to ensure good heat dissipation. It can be widely used in electronic countermeasures, broadband communication and other fields.

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Pressure Range (V_{GG})	-6 to 0V
Gate Current (I_G)	4mA
Channel Temperature (T_{CH})	275 ℃
Peak Welding Temperature (< 5s)	320 ℃

Note:Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V
Drain Static Current (I_{DQ})	900mA
Gate Voltage (V_{GG})	2.1 V
Channel Temperature (T_{CH})	225 ℃
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

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Power-on Sequence

1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 4A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}), so that the drain current is 900mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal.
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage;

Note: When the circuit is designed, a timing protection circuit is needed to power off the bias voltage, to ensure that the V_{GG} is fully powered on and then add V_{DD}, to ensure that the V_{DD} is reduced to below 5V when powering off the V_{GG}, to start powering off the V_{GG}; Especially in T_{DD} applications, gate supply decoupling capacitors need to be rigorously evaluated to meet the switching speed requirements.

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ESD WRANING

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Electrical Specifications

Parameters	Test Conditions	Min.	Typ.	Max.	Units
Gain	2GHz	-	23.02	-	dB
	3GHz	-	24.07	-	dB
	4GHz	-	22.86	-	dB
	5GHz	-	23.91	-	dB
	6GHz	-	23.24	-	dB
Input Return Loss	2GHz	-	-16.97	-	dB
	3GHz	-	-17.89	-	dB
	4GHz	-	-36.69	-	dB
	5GHz	-	-10.42	-	dB
	6GHz	-	-17.18	-	dB
Output Return Loss	2GHz	-	-22.28	-	dB
	3GHz	-	-17.75	-	dB
	4GHz	-	-13.22	-	dB
	5GHz	-	-20.82	-	dB
	6GHz	-	-10.28	-	dB
Psat	2GHz	-	42.64	-	dBm
	3GHz	-	44.72	-	dBm
	4GHz	-	44.71	-	dBm
	5GHz	-	44.91	-	dBm
	6GHz	-	44.61	-	dBm
PAE	2GHz	-	30.12	-	%
	3GHz	-	41.20	-	%
	4GHz	-	32.09	-	%
	5GHz	-	39.87	-	%
	6GHz	-	33.59	-	%
Saturation Power Gain	2GHz	-	12.32	-	dB
	3GHz	-	16.31	-	dB

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	4GHz	-	16.01	-	dB
	5GHz	-	19.01	-	dB
	6GHz	-	17.61	-	dB
Operating Voltage	-	-	28	-	V

S parameter test conditions: Temp=+25℃, V_{DD}=+28V, I_{DQ}=900mA;

Psat test conditions; Temp =+25℃,V_{DD} =+28V, I_{DQ}=50mA, 100us pulse width, period 1ms pulse wave test;

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Typical Performance (EVB test data, 2GHz ~ 6GHz)

Parameters	Typ.									Units
Frequency	2000	2500	3000	3500	4000	4500	5000	5500	6000	MHz
Gain	23.02	24.38	24.07	23.34	22.86	22.98	23.91	24.47	23.24	dB
Input Return Loss	-16.97	-29.08	-17.89	-18.91	-36.69	-14.11	-10.42	-11.21	-17.18	dB
Output Return Loss	-22.28	-21.85	-17.75	-16.05	-13.22	-12.91	-20.82	-12.53	-10.28	dB
Output Power @P_{sat}	42.64	44.29	44.72	44.50	44.71	44.61	44.91	44.24	44.61	dBm
Power Gain @P_{sat}	12.32	14.49	16.31	14.89	16.01	17.31	19.01	18.54	17.61	dB
PAE@P_{sat}	30.12	40.57	41.20	33.24	32.09	31.96	39.87	37.69	33.59	%

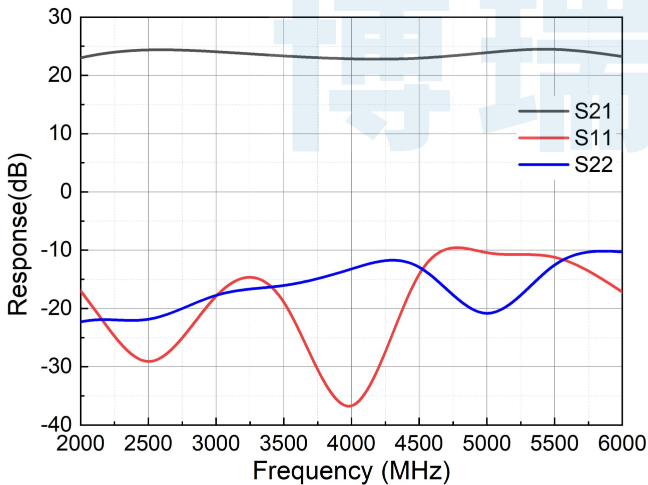
S parameter test conditions: Temp =+25°C, V_{DD}=+28V, I_{DQ}=900mA;

Psat test conditions; Temp =+25°C, V_{DD}=+28V, I_{DQ}=50mA, 100us pulse width, period 1ms pulse wave test;

Input and output characteristics test conditions: Temp =+25°C,V_{DD} =+28V, I_{DQ}=900mA, 100us pulse width, period 1ms pulse wave test;

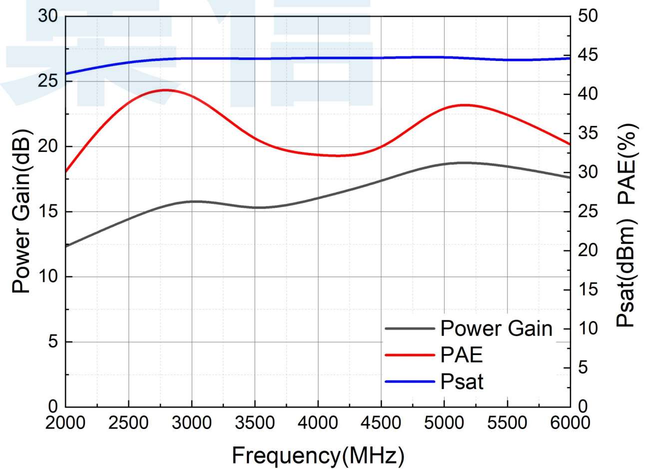
Note: P_{sat} defined as the saturation power output of the evaluation board.

Typical Performance (Temp =+25°C)



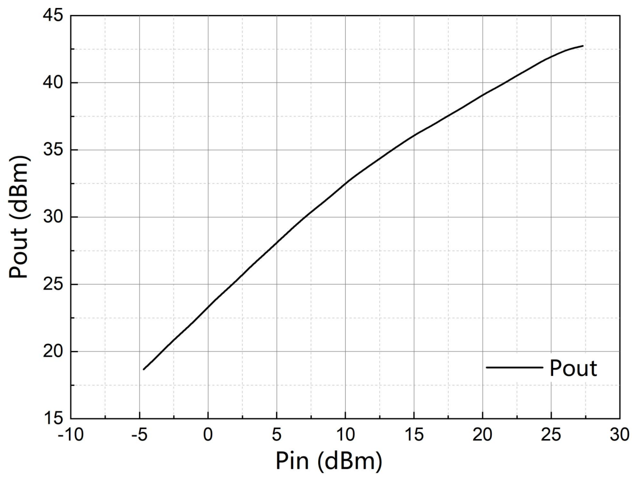
Gain & Input Return Loss & Output Return Loss vs. Freq

V_{DD}=+28V, I_{DQ}=900mA



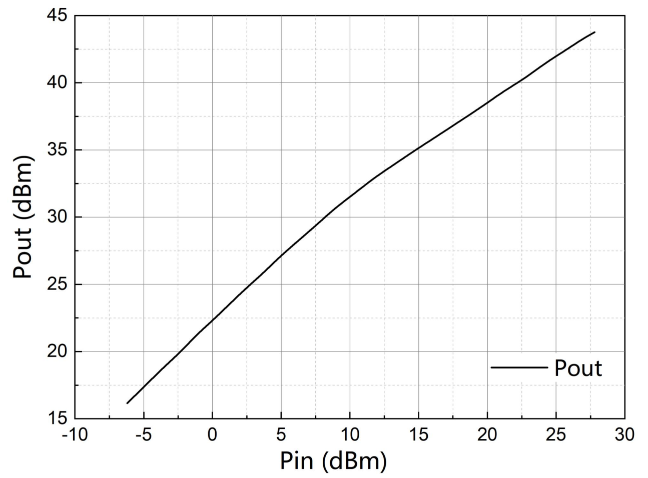
Psat & PAE vs. Freq

I_{DQ}=50mA, pulse wave test



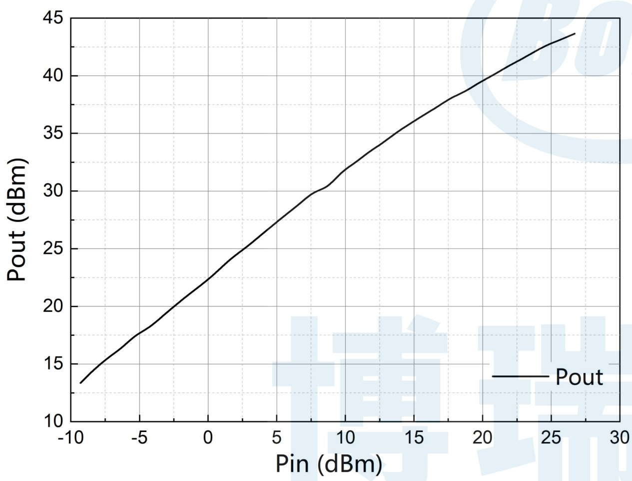
P_{out} vs. P_{in} @2GHz

I_{DQ}=900mA, pulse wave test



P_{out} vs. P_{in} @4GHz

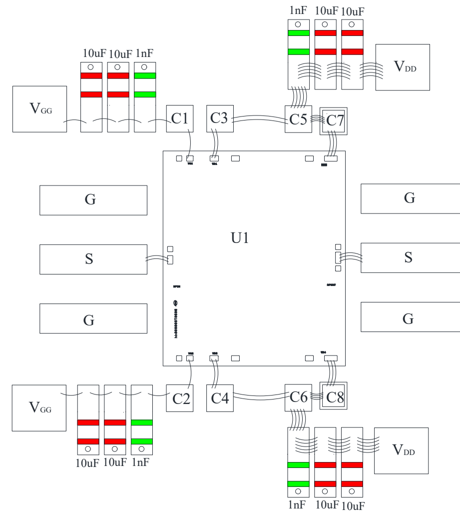
I_{DQ}=900mA, pulse wave test



P_{out} vs. P_{in} @6GHz

I_{DQ}=900mA, pulse wave test

Typical Application Schematic and Assembly Diagram



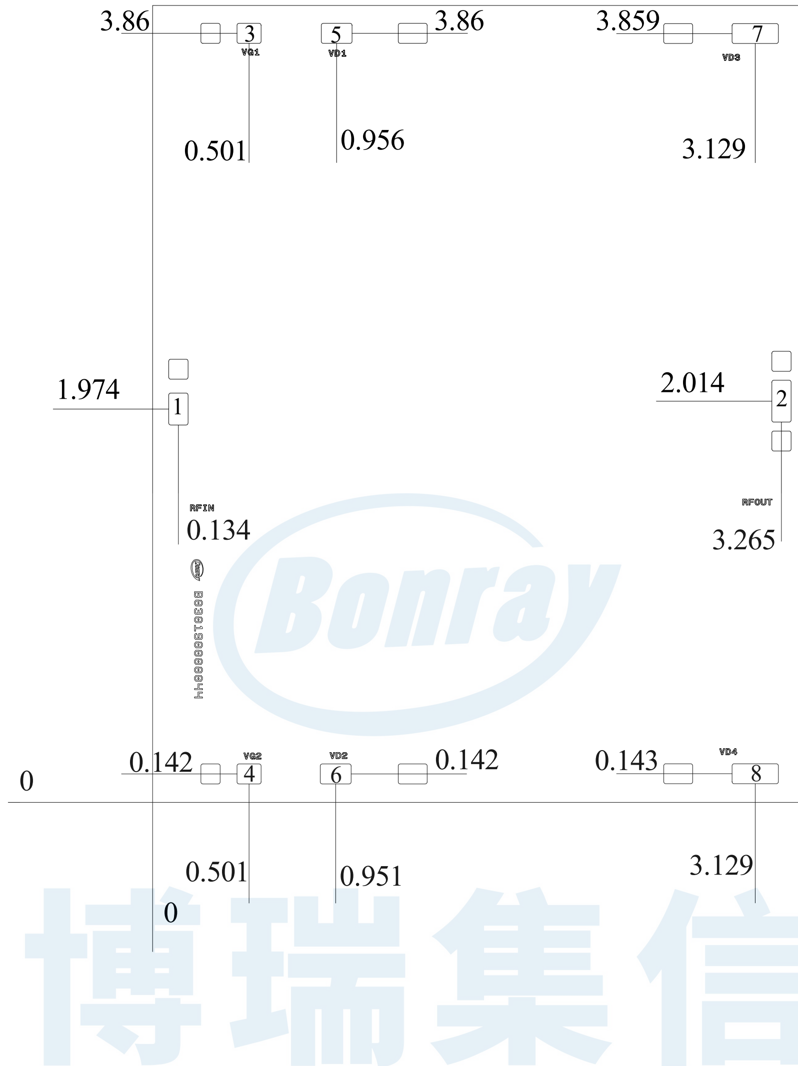
Bill of Material

Designator	Package	Description	Part Numbrer
U1	3.4 mm * 4 mm	/	BRGF060020LD
C1,C2,C3,C4,C5,C6	0.5 mm * 0.5 mm * 0.35 mm	1000pF	CT91202X102M100TW
C7,C8	0.508 mm * 0.508 mm * 0.15 mm	100pF	SG201N101MSTW

Handling Precautions:

1. **Storage:** The chip must be placed in a container with electrostatic protection function, and stored in a nitrogen environment.
2. **Cleaning treatment:** The bare chip must be operated and used in a clean environment. It is forbidden to use liquid cleaning agent to clean the chip.
3. **ESD prevention:** Strictly comply with the requirements of ESD prevention to avoid electrostatic damage.
4. **Routine operation:** Use vacuum pen or precision pointed tweezers to pick up the chip. Avoid touching the chip surface with tools or fingers during operation.
5. **Installation operation:** The chip installation needs to use AuSn solder eutectic sintering process, the mounting surface must be clean and flat, and the gap between the chip and the input and output RF connection line substrate is as small as possible.
6. **Sintering process:** with 80/20AuSn sintering, it is recommended that the peak temperature of sintering is 300℃, and the sintering duration is about 5 seconds.
7. **Bonding operation:** no special Notes, recommended 25μm gold wire wedge welding process, thermoultrasonic bonding temperature recommended 150℃.
8. **Power-on sequence:** The power-on and power-off sequence must be followed.
9. The hollow rate of adhesive sheet: not more than 5%.
10. Please contact customer service if you have any questions.

Mechanical Information（Units：mm）



Notes:

1. The back of the chip gold-plated;

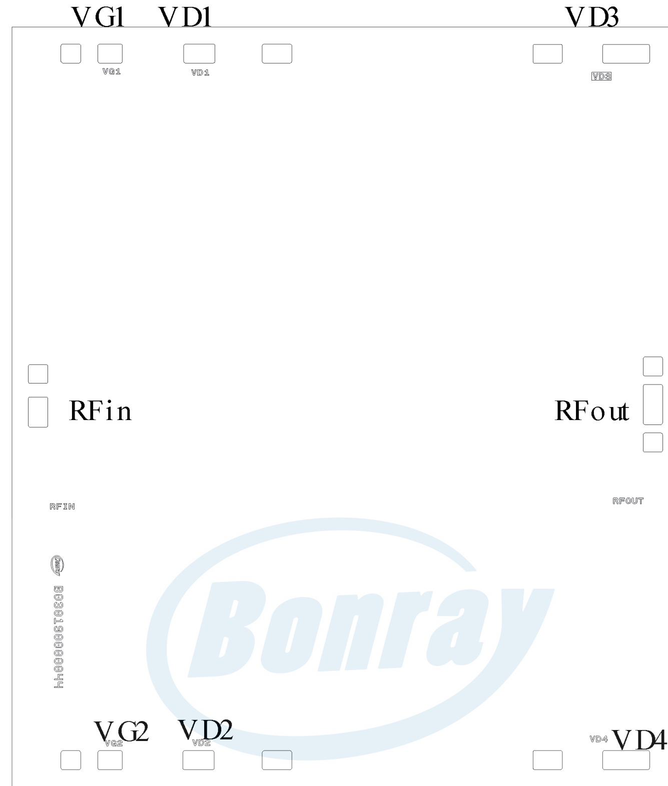
2. The back of the chip is grounded;

3. Bonding pressure point gold-plated, pressure point size: RFin pressure point: 100um×160um; RFout pressure point: 100um×210um; VG1 pressure point: 125um×100um; VG2 pressure point: 125um×100um; VD1 pressure point: 160um×100um; VD2 pressure point: 160um×100um; VD3 pressure point: 240um×100um; VD4 pressure point: 240um×100um;

4. Can not be bonded on the through hole;

5. Overall size tolerance: ±30um.

Leading End Arrangement



Pad Description

Symbol	Features
RFin	RF Input matched to 50 ohms;
RFout	RF Output matched to 50 ohms;
VG1/VG2	Gate supply voltage port.
VD1/VD2	First stage drain supply voltage port.
VD3/VD4	Second level drain supply voltage port.
Backside	The back of the chip is grounded, and this pin and package substrate must be connected to the RF/DC ground.

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