Product Features

Frequency: DC ~ 4GHz

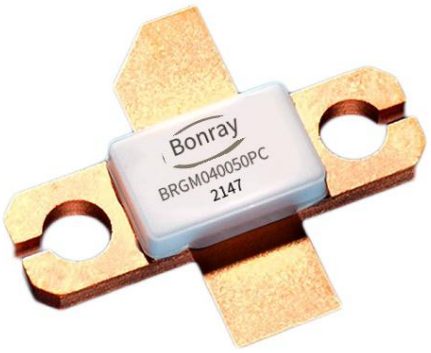
Gain : 19.2dB@0.95GHz

Psat: 48.3dBm@0.95GHz

PAE: 57.1% (0.95GHz,Pout=48.3dBm)

Operation Voltage: 28V, I_{DQ} 310mA

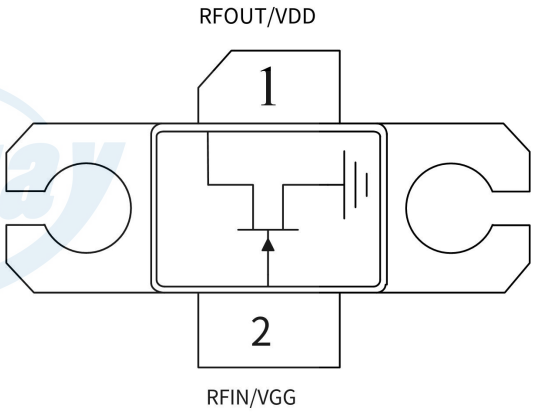
Package: PC (ceramic seal)



General Description

The BRGM040050PC is an wideband transistor designed using the GaN HEMT process to achieves 50W (47dBm) output in the DC to 4GHz with a power add efficiency of 50%.The power amplifier has the characteristics of high efficiency, high gain and wide bandwidth. This makes the product has a strong application ability in both linear and compressed amplifier circuits, and also simplifies link design and related heat consumption management.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGM040050PC	PC	DC ~ 4GHz 50W GaN Transistor

Applications

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

Commercial and Military Radars

Universal Transmitters and Jammers

Ultrashort Wave Communication Equipment

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain current (I_D)	6A
Gate Current (I_G)	14mA
Continuous Dissipated Power (P_D)	75W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note:Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	310mA (Typ)
Gate Voltage (V_{GG})	-2.59V (Typ)
Channel Temperature (T_{CH})	225 ° C (Max)
Continuous Dissipated Power CW (P_D)	60W (Max)
Storage Temperature	-65℃ to +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, T_A =25℃, V_{DD}=+28V,I_{DQ}=310mA, Fre=1GHz, CW, P_{out}=50W

Thermal parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	3.3	℃/W
Channel temperature (T_{ch})		225	℃

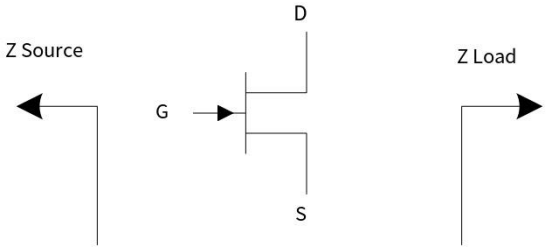
Note: θ_{JC} to measure the thermal resistance to the bottom of the package;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

Radio Frequency Features (Load Pull Data)



Optimum Power Matching

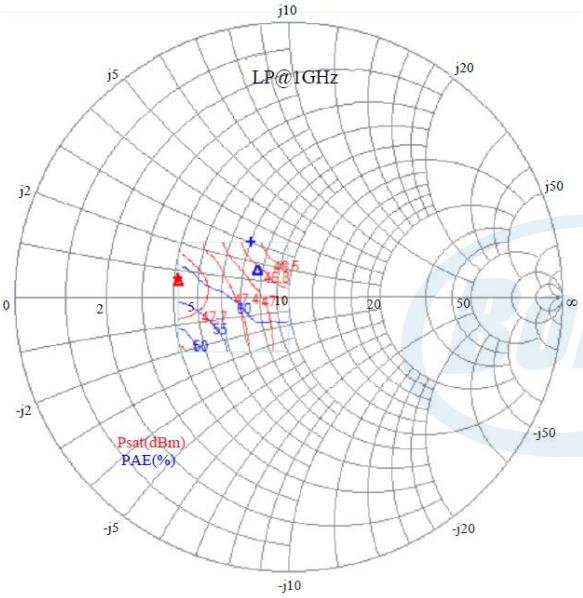
Load Pull Data -- Optimal Power Matching					
Parameters	**Typ.**				**Units**
Frequency	1000	2000	3000	4000	MHz
Z_{source}	2.24 * 2.58 j	1.85 * 4.04 j	1.96 * 9.51 j	2.71 * 11.7 j	Ω
Z_{load}	4.25 * 0.68 j	3.89 * 3.02 j	4.58 * 4.54 j	4.15 * 6.32 j	Ω
$I_D@P_{sat}$	4.03	4.4	4.1	4.3	A
$OutputP_{sat}$	48.43	48.5	48.4	48.5	dBm
$PAE@P_{sat}$	60.9	55.28	63	58.5	%
Power Gain $@P_{sat}$	19.01	14.09	16	15.5	dB
Test Conditions: Temp=+25℃, V_{DD}=+28V, I_{DQ}=310mA, CW;					

Optimum Efficiency Matching

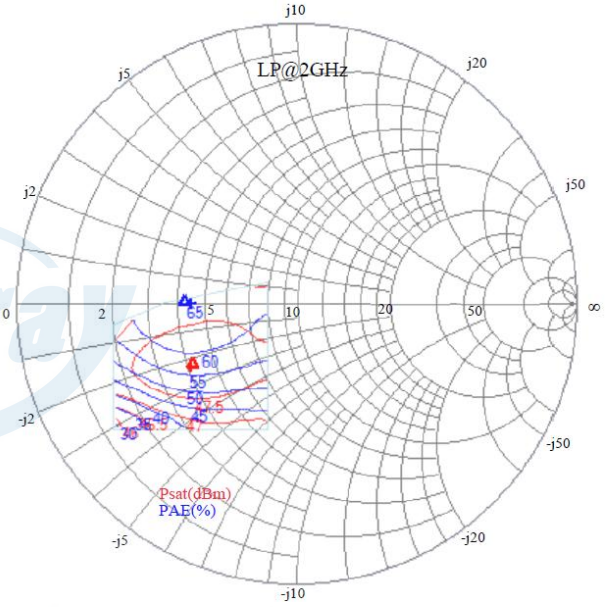
Load Pull Data -- Best Efficiency Matching					
Parameters	**Typ.**				**Units**
Frequency	1000	2000	3000	4000	MHz
Z_{source}	2.24 * 2.58 j	1.85 * 4.04 j	1.96 * 9.51 j	2.71 * 11.7 j	Ω
Z_{load}	7.12 * 3.01 j	3.6 + j * 0.69	2.69 * 2.6 j	2.87 * 6.07 j	Ω
$I_D@P_{sat}$	3.71	2.16	3.0	2.71	A
$OutputP_{sat}$	48.36	46.16	48	47.5	dBm
$PAE@P_{sat}$	64.66	65.86	72.7	72.4	%
Power Gain $@P_{sat}$	17.47	14.5	16	13.9	dB
Test Conditions: Temp =+25℃, V_{DD}=+28V, I_{DQ}=310mA, CW					

Load Pull Smith

power amplifier typically displays different RF input and output characteristics in a specific impedance environment.due to their own characteristics. The impedance of the device here is the peripheral RF impedance of the amplifier or the impedance of the Load-Pull system rather than the impedance of the amplifier itself. The relevant impedance points can be selected and designed by referring to the contours of Smith circle diagram to ensure the high power and high efficiency of the amplifie



High Impedance Circle Diagram of 1GHz

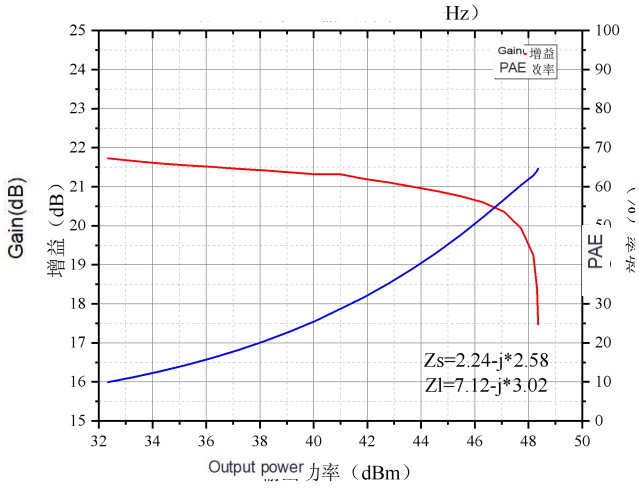


High Impedance Circle Diagram of 2GHz

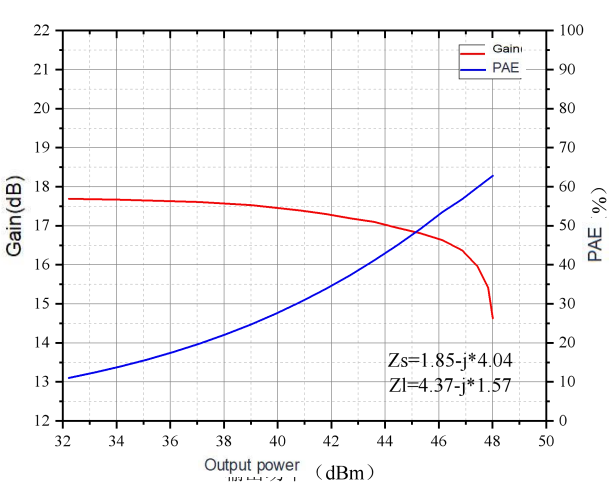
Notes:

1. The central impedance of the Smith circle diagram above is Zo=10Ω;
2. The contour interval of the red line Pout in the Smith circle diagram is 0.5dB, and the PAE interval is 5%;
3. The test conditions are as follows: Temp =+25℃, V_{DD}=28V, I_{DQ}=310mA, CW wave test;

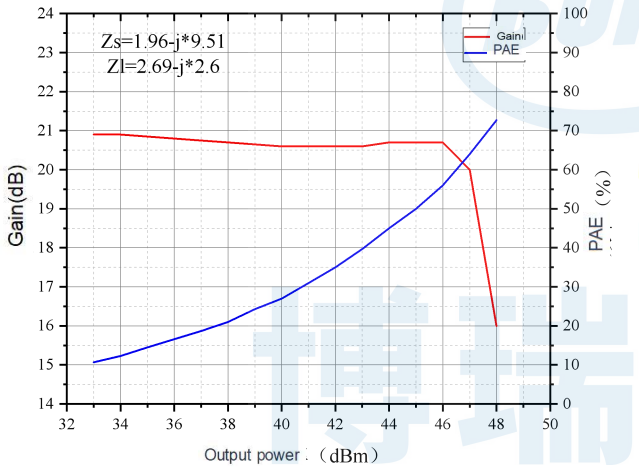
Typical Performance (Load Pull data, Temp =+25℃, V_{DD}=+28V, I_{DQ}=310mA, CW)



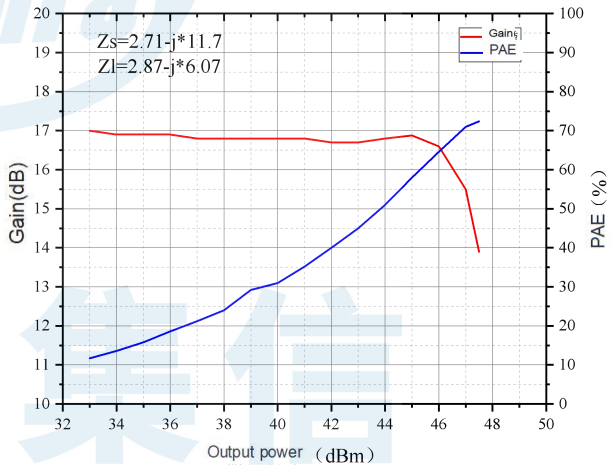
Gain, PEA vs. Pout @1GHz



Gain, PEA vs. Pout @2GHz



Gain, PEA vs. Pout @3GHz



Gain, PEA vs. Pout @4GHz

Typical Performance (Evaluation board data)

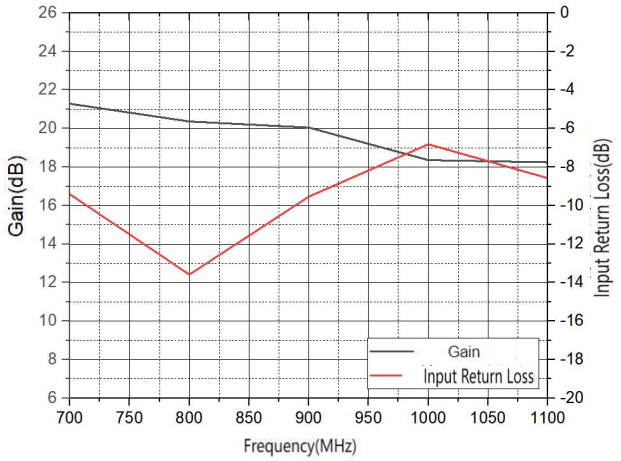
Evaluation Board (0.7GHz ~ 1.1GHz) Test Data						
Parameters	**Typ.**					**Units**
Frequency	700	800	900	1000	1100	MHz
Gain	21.3	20.4	20.1	18.4	18.2	dB
Small Signal Input Return Loss	-9.4	-13.6	-9.5	-6.8	-8.6	dB
Drain Current @P_{sat}	3.43	4.05	4.16	4.19	3.17	A
Pout (dBm) @P_{sat}	47.2	47.3	47.8	48.8	48.1	dBm
Pout (dBm) @P_{sat}	52.5	53.7	60.3	75.9	64.6	W
PAE@P_{sat}	53.1	46.3	50.0	62.9	69.3	%
Power Gain @P_{sat}	15.6	15.1	15.1	14.5	14.4	dB
Test Condition: Temp =+25℃, V_{DD}=+28V, I_{DQ}=310mA, CW						

Note: P_{sat} defined as the maximum power output of the evaluation board;

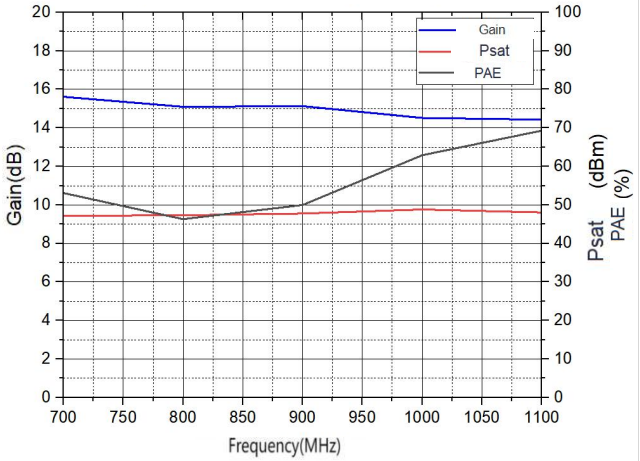
Wide Voltage Characteristics (Evaluation board data)

Evaluation Board (0.7GHz ~ 1.1GHz) Test Data				
Parameters	**Typ.**			**Units**
Frequency	700	900	1100	MHz
Output Power @P_{sat}	48.1	48.3	48.7	dBm
Output Power @P_{sat}	64.6	67.6	74.1	W
Drain Current @P_{sat}	3.74	4.45	3.54	A
PAE@P_{sat}	54.3	47.4	66.0	%
Gain @P_{sat}	12.96	14.14	13.65	dB
Test Conditions: Temp =25℃, =+32V, =310mA, CW $V_{DD}I_{DQ}$				

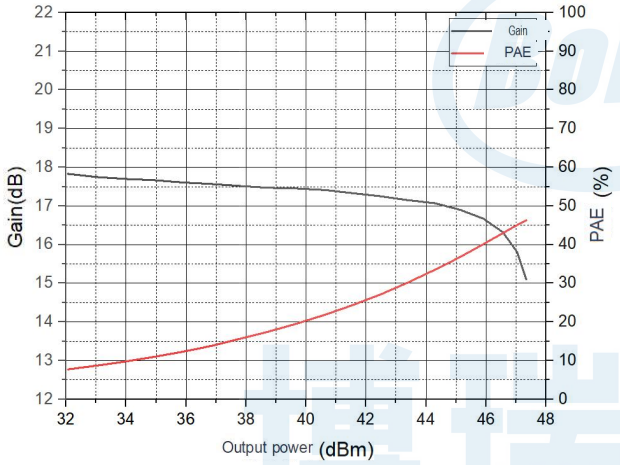
Typical Performance (Evaluation board: 0.7GHz-1.1GHz, Temp =+25℃, V_{DD}=+28V, =I_{DQ}310mA, CW)



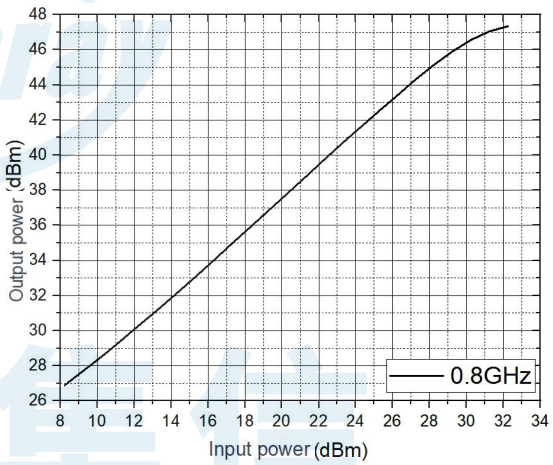
Standing Wave, Gain vs. Freq@25℃



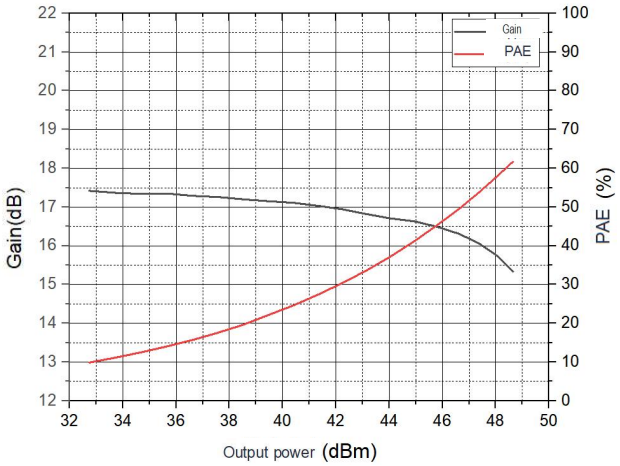
Gain,Psat,PEA vs. Freq@25℃



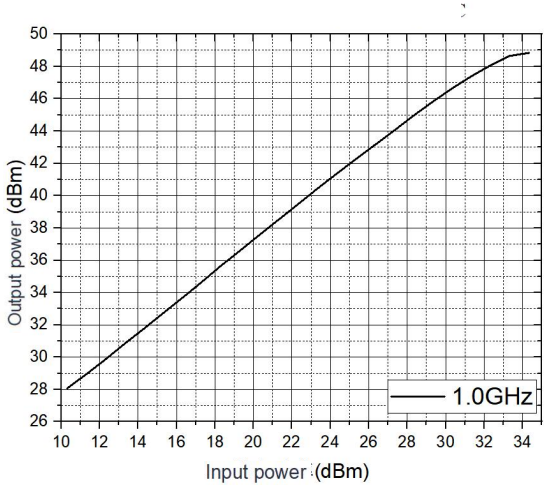
Gain, PEA vs. P_{out} @0.8GHz



P_{out} vs. P_{in}@0.8GHz

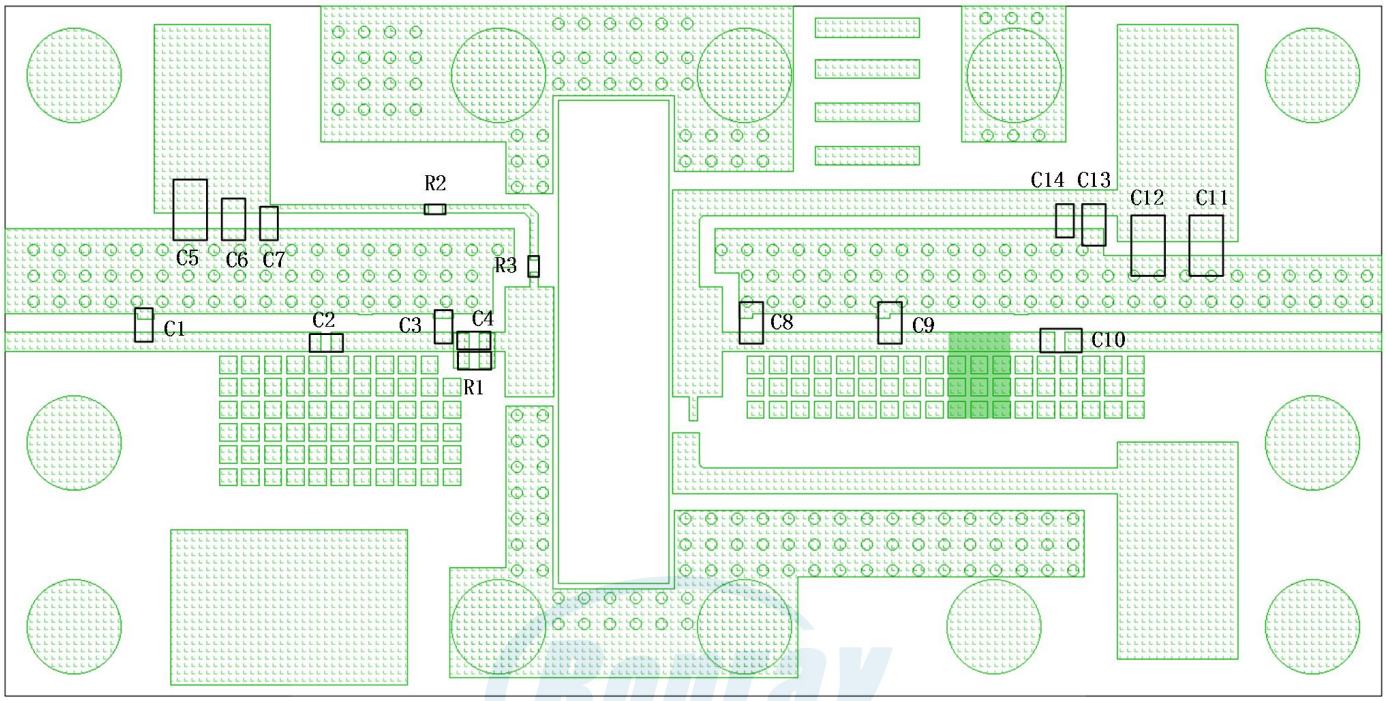


Gain, PEA vs. P_{out} @1GHz



P_{out} vs. P_{in}@1GHz

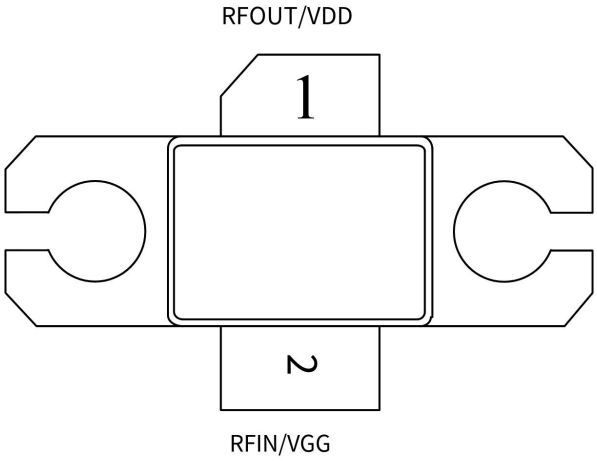
PCB Evaluation Board



Bill of Material

Number	Designator	Description	Package	Quantity
1	C1	CAP, 4.3 pF, 50 VDC	C0603	1
2	C2	CAP,82pF,50VDC	C0603	1
3	C3	CAP,10pF,50VDC	C0603	1
4	C4	CAP, 0.5 pF, 50 VDC	C0603	1
5	C5,C11,C12	CAP,10uf, 50VDC	C1210	3
6	C6,C13	CAP, 0.1 uF, 50 VDC	C0805	2
7	C7,C14	CAP,1nF,50VDC	C0603	2
8	C8	CAP,10pF,200VDC	C0603	1
9	C9	CAP, 4.7 pF, 200 VDC	C0603	1
10	C10	CAP,82pF,50VDC	C0805	1
11	R3	RES,1Ohm	R1206	1
12	R1	RES, 5.6 Ohm	R0603	1
13	R2	RES,36Ohm	R0603	1

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V_{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

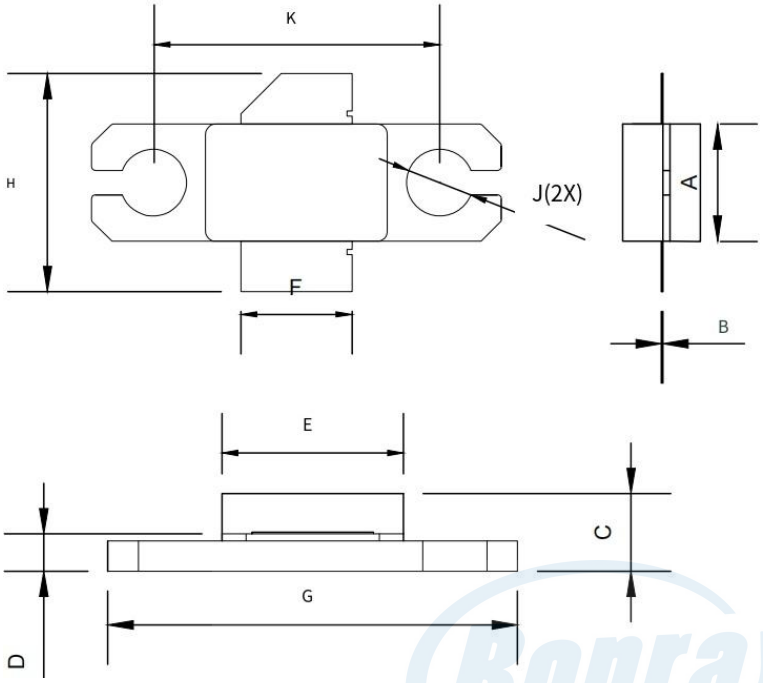
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 8A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 310mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	5.675	5.800	5.925
B	0.120	0.125	0.130
C	4.12	4.375	4.63
D	2.10	2.15	2.20
E	8.84	9.00	9.04
F	5.375	5.50	5.625
G	20.175	20.30	20.425
H	10.30	10.80	11.30
J	3.175	3.30	3.425
K	14.075	14.20	14.325

Recommended Soldering Temperature Profile