Product Features

Frequency: DC ~ 6GHz

Gain: 20.5dB@1.6GHz

Psat: 38.1dBm@1.6GHz

PEA: 66.1% (Pout=38dBm, 1.6GHz)

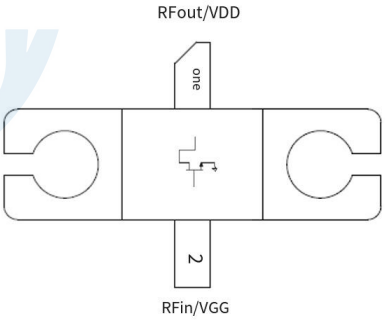
Operation Voltage: 28V, I_{DQ} 100mA

Package: PG (ceramic seal)

General Description

The BRGM060006PC is an wideband transistor designed using the GaN HEMT process to achieves 6W (37.8dBm) output in the DC to 6GHz with a power added efficiency of 66.10%. The power amplifier has the characteristics of high efficiency, high gain and wide bandwidth. This makes the product has a strong application ability in both linear and compressed amplifier circuits, and also simplifies link design and related heat consumption management.

Functional Block Diagram



Ordering Information

Part	Package	Description
BRGM060006PGD	PG	DC ~ 6GHz 6W GaN Transistor

Applications

Power Amplification Stage for Wreless Infrastructure

Test and Measurement Equipment

Commercial and Military Radars

Universal Transmitters and Jammers

Ultrashort Wave Communication Equipment

Absolute Maximum Ratings

Parameters	Values
Gate drain breakdown voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain current (I_D)	1.1 A
Gate current (I_G)	2mA
Continuous dissipated power (P_D)	25W
Channel temperature (T_{CH})	275 ℃
Mounting temperature (30 seconds)	245 ℃

Note: The absolute maximum rating indicates the limit value that the device can withstand, exceeding the absolute maximum rating may cause permanent damage to the device. Working under absolute maximum rating conditions for a long period of time will affect the reliability of the device. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain voltage (V_{DD})	+28V (Typ)
Drain static current (I_{DQ})	100mA (Typ)
Gate voltage (V_{GG})	-2.52V (Typ)
Channel temperature (T_{CH})	225 ° C (Max)
Continuous dissipated power CW (P_D)	20W (25 ° C)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +85℃

Note:The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, T_A=25℃, V_{DD}=+28V, I_{DQ}=100mA, Freq=1GHz, CW wave, P_{out}=6W

Thermal Parameters

Parameters	Test Conditions	Value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	TBD	℃/W
Channel temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the package

ESD Warnings

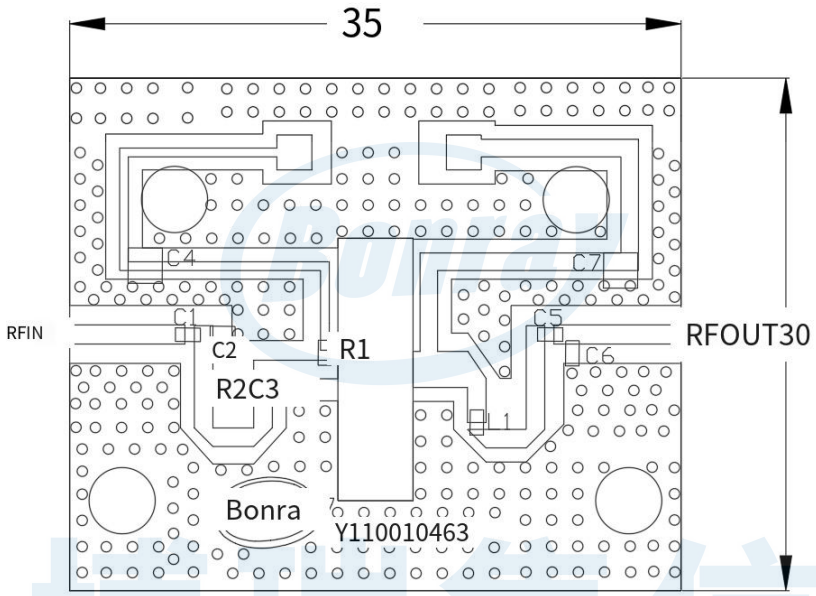
ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

Option 1: EVB Test Data (0.8GHz~1.8GHz, V_{DD}=28V, I_{DQ}=100mA, single tone signal)

Frequency	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	MHz
Gain	20.1	19.9	19.7	19.6	19.7	19.8	20.2	20.7	21.4	21.8	21.9	dB
Psat	37.7	37.85	38.4	38.55	38.75	38.7	38.7	38.35	38.3	38.5	38.85	dBm
PAE@P_{sat}	46.9	47.8	47.7	46.6	49.6	50.8	52.2	49.6	52.1	55.1	57.1	%
Power Gain	13.7	14.6	13.5	12.2	12.4	13.2	14.8	15.2	15.6	16.5	15	dB

PCB Evaluation Board

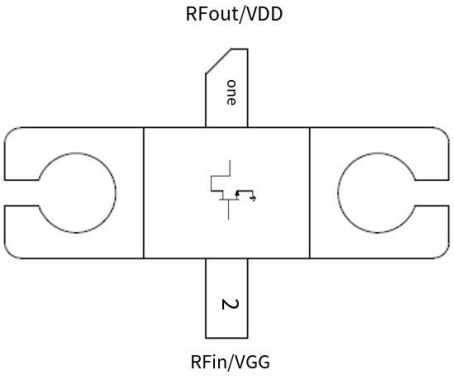


Bill of Material

Reference Designator	Value	Package Size	Kind
C1, C5	27pF	0603	Capacitors
C2	1.8 pF	0603	Capacitors
C3	20pF	0603	Capacitors
C4, C7	10uF	1210	Capacitors
C6	0.75 pF	0603	Capacitors
R1	50ohm	0603	Resistor
R2	8.2 ohm	0603	Resistor
L1	1.8 nH	0603	Inductance

Note: PCB is 20mil Rogers 4350 sheet

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain, drain voltage input, RF power signal 50Ω system output;
2	RFin/V_{GG}	Gate, gate voltage regulation, RF signal 50Ω system input;
-	Package Base	Ground substrate, which needs to be welded to the substrate under the card opening window;

Power-on Sequence

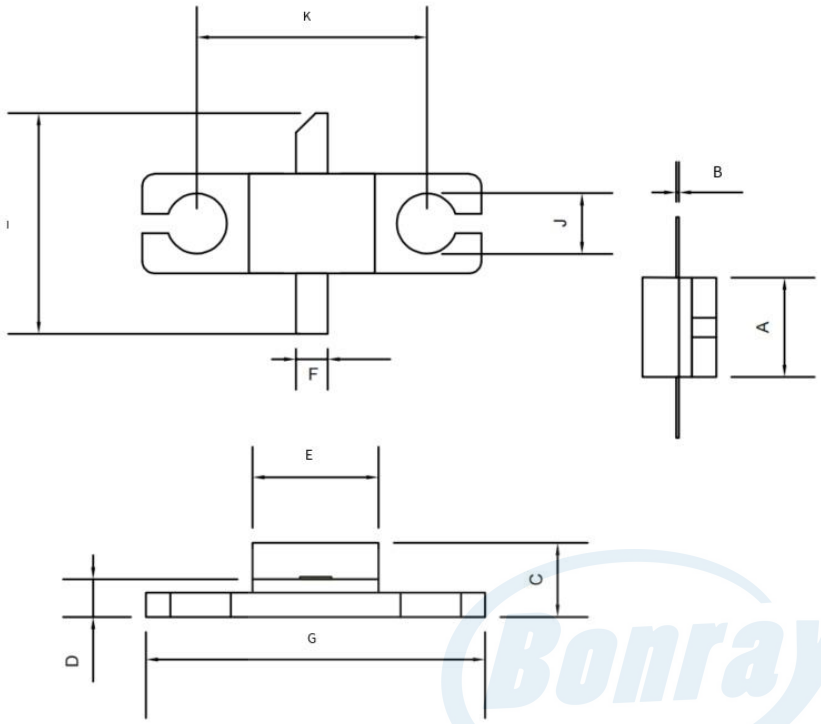
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 2A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 100mA;
6. Input RF signal;

Power-off Order

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage;
4. Turn off the gate Supply Voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Dim	Units : mm		
	Min	Typ	Max
A	4	4.1	4.2
B	0.05	0.1	0.15
C	2.9	3.15	3.4
D	1.4	1.55	1.7
E	5.05	5.2	5.35
F	1.25	1.3	1.35
G	13.9	14	14.1
H	9.7	10	10.3
J	2.42	2.5	2.58
K	9.45	9.5	9.55

Recommended Soldering Temperature Profile