Features

Frequency: DC ~ 6GHz

Gain: 18.4dB@1.3GHz

Psat: 42.1dBm@1.3GHz

PEA: 70%(Pout=42.1dBm, 2GHz)

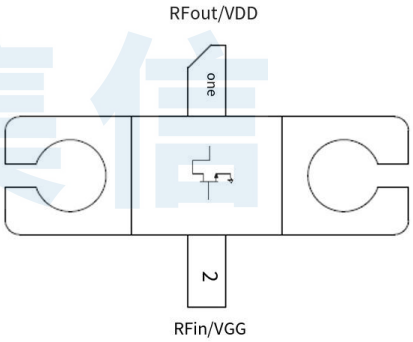
Operation Voltage: 28V, I_{DQ} 200mA

Package : PG (ceramic seal)

General Description

The BRGM060015PG is an wideband power amplifier designed using the GaN HEMT process to achieves 15W output in the DC to 6GHz with a power efficiency of 70%. The power amplifier has the characteristics of high efficiency, high gain and wide bandwidth. This makes the product has a strong application ability in both linear and compressed amplifier circuits, and also simplifies link design and related heat consumption management. In order to facilitate user installation and use, this product adopts PG flanged package form.

Functional Block Diagram



Ordering Information

Part	Package	Description
BRGM060015PG	PG	DC ~ 6GHz 15W GaN Transistor

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	2.1 A
Gate current (I_G)	4mA
Continuous Dissipated Power (P_D)	29W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Working Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	200mA (Typ)
Gate Voltage (V_{GG})	-2.35V (Typ)
Channel Temperature (T_{CH})	225 ° C (Max)
Continuous Power Dissipation CW (P_D)	25W (Max)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, T_A =25℃, V_{DD} =+28V, I_{DQ} =200mA, Fre=1GHz, CW wave, P_{out}=15W

Thermal parameters

Parameters	Test Condition	Value	Units
Thermal resistance (θ_{JC})	Continuous wave mode tested at 70 ° C	5.6	℃/W
Channel temperature (T_{ch})		225	℃

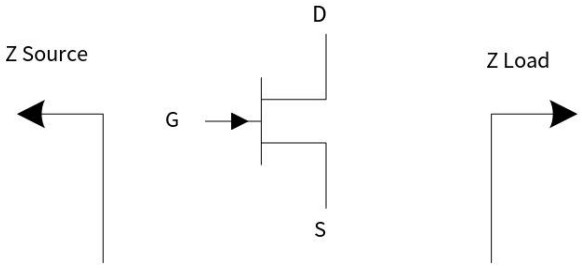
Note: $\boldsymbol{\theta_{JC}}$ For measuring the thermal resistance to the bottom of the package.

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

Radio Frequency Features (Load Pull Data)



Optimum Power Matching

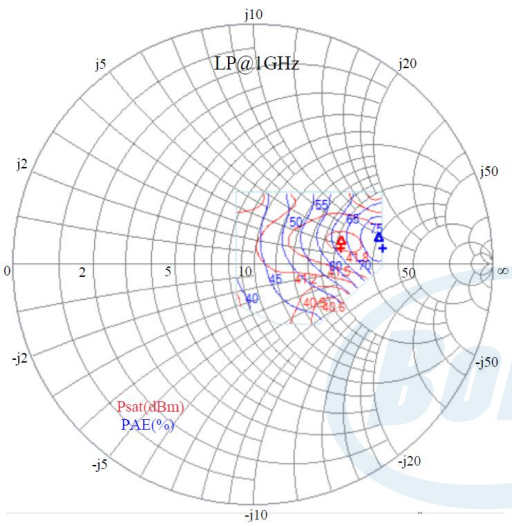
Load Pull Data --Optimal Power Matching							
Parameters	**Typ.**						**Units**
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	4.21 + j * 16.42	2.58 + j * 2.39	2.73 * 7.16 j	3.64 * 13.01 j	1.6 * 18.74 j	1 - j * 5.26	Ω
Z_{load}	34.08 * 1.49 j	13.8 * 5.12 j	16.37 * 6.37 j	12.98 * 10.79 j	14.61 * 19.38 j	10.62 * 8.73 j	Ω
$I_D@P_{sat}$	0.74	1.3	1.23	1.09	1.07	1.15	A
$OutputP_{sat}$	42.36	42.88	43.09	42.47	43	43.15	dBm
$PAE@P_{sat}$	82.41	52.33	56.56	54.08	65.8	61.69	%
Gain $@P_{sat}$	23.59	17.63	13.85	12.31	11.4	13.7	dB
Test Conditions: Temp=+25℃, =+28V, =200mA, CW wave test;$V_{DD}I_{DQ}$							

Optimum Efficiency Matching

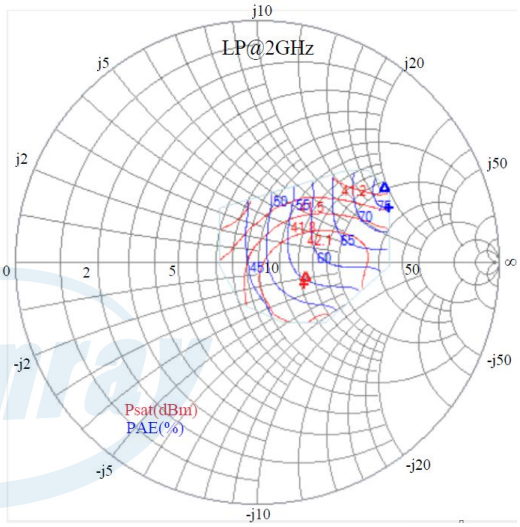
Load Pull Data -- Best Efficiency Matching							
Parameters	**Typ.**						**Units**
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	4.21 + j * 16.42	2.58 + j * 2.39	2.73 * 7.16 j	3.64 * 13.01 j	1.6 * 18.74 j	1 - j * 5.26	Ω
Z_{load}	33.25 + j * 6.03	20.73 + j * 20.27	7.77 + j * 9.12	7.91 * 4.31 j	8.76 * 11.92 j	10.62 * 8.73 j	Ω
I_D@P_{sat}	0.68	0.55	0.49	0.68	0.94	0.76	A
OutputP_{sat}	42.22	40.97	40.19	41.18	42.5	41.5	dBm
PAE@P_{sat}	87.37	80.15	73.55	65.67	69.2	66.5	%
Gain @P_{sat}	23.17	17.52	14.27	13.44	12	13.7	dB
Test Conditions: Temp =+25°C, =+28V, =200mA, CW wave test;$V_{DD}$$I_{DQ}$							

Load Pull Smith

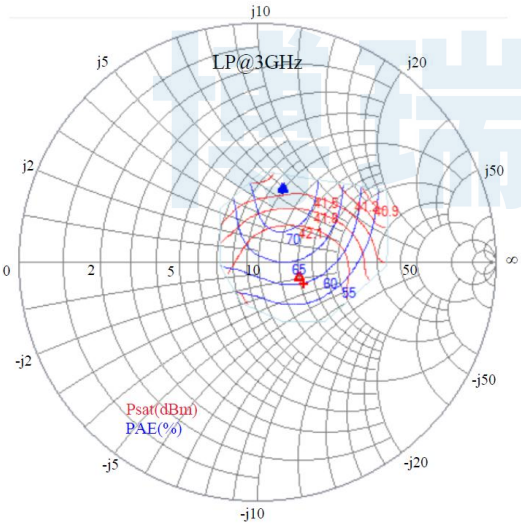
power amplifier typically displays different RF input and output characteristics in a specific impedance environment.due to their own characteristics. The impedance of the device here is the peripheral RF impedance of the amplifier or the impedance of the Load-Pull system rather than the impedance of the amplifier itself. The relevant impedance points can be selected and designed by referring to the contours of Smith circle diagram to ensure the high power and high efficiency of the amplifie.



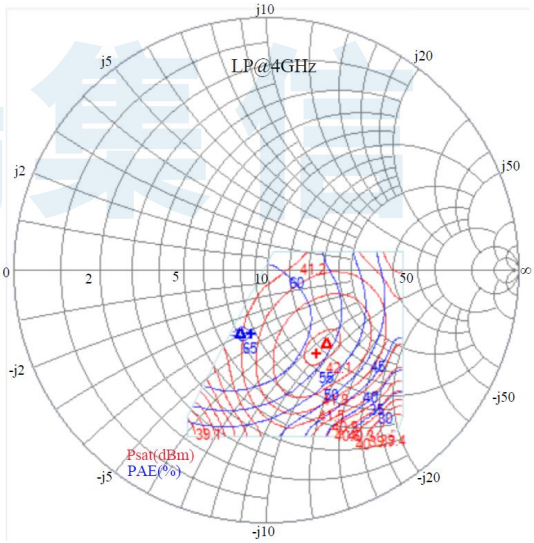
High Impedance Circle Diagram of 1GHz



High Impedance Circle Diagram of 2GHz



High Impedance Circle Diagram of 3GHz

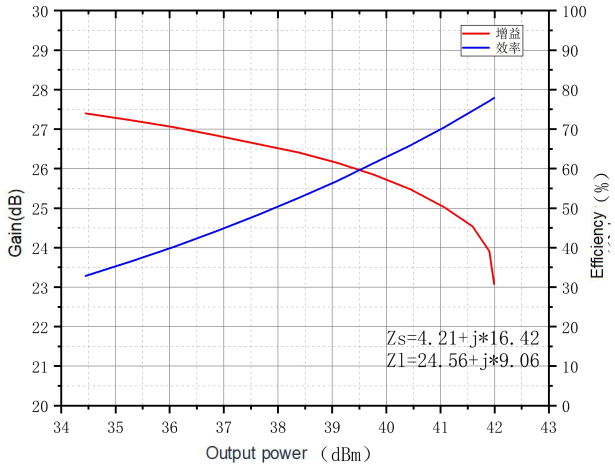


High Impedance Circle Diagram of 4GHz

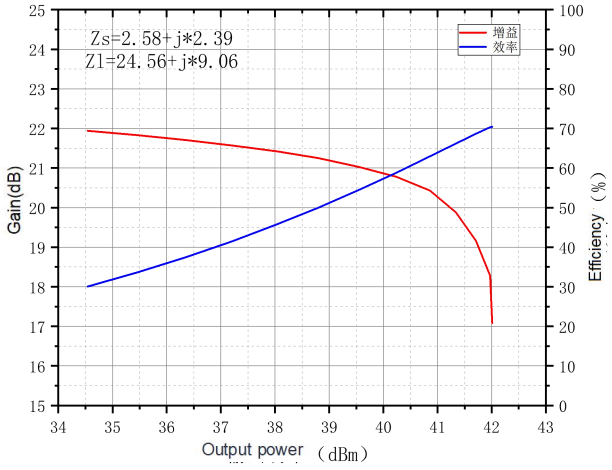
Notes:

1. The central impedance of the Smith circle diagram above is Zo=10Ω;
2. The contour interval of the red line Pout in the Smith circle diagram is 0.3dB, and the PAE interval is 5%;
3. The test conditions are: =28V, =200mA, Temp=+25℃, CW wave test;V_{DD} I_{DQ}

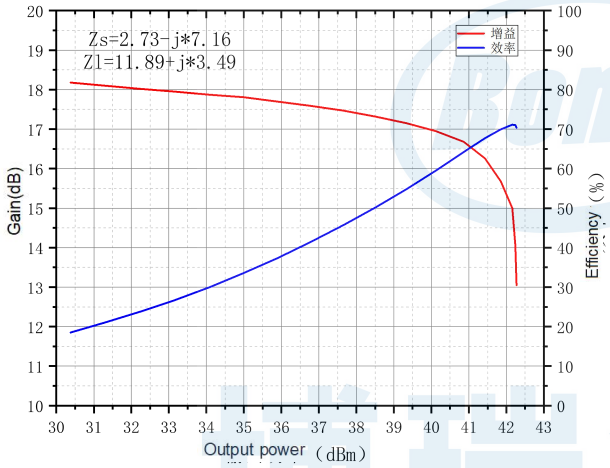
Typical Performance (Load Pull data, V_{DD}=+28V, I_{DQ}=200mA, Temp=+25℃, CW wave test)



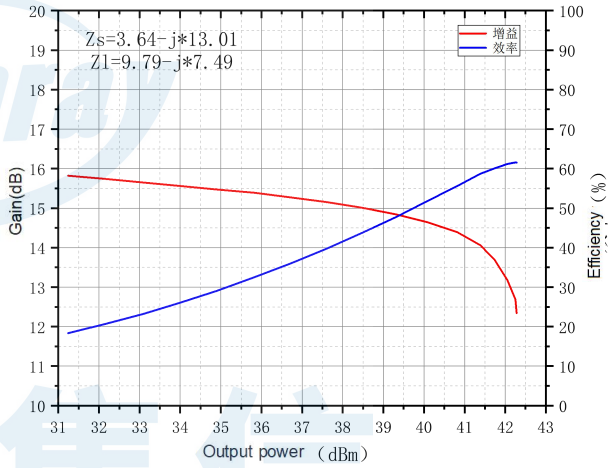
1GHz Gain, Efficiency vs. P_{out}



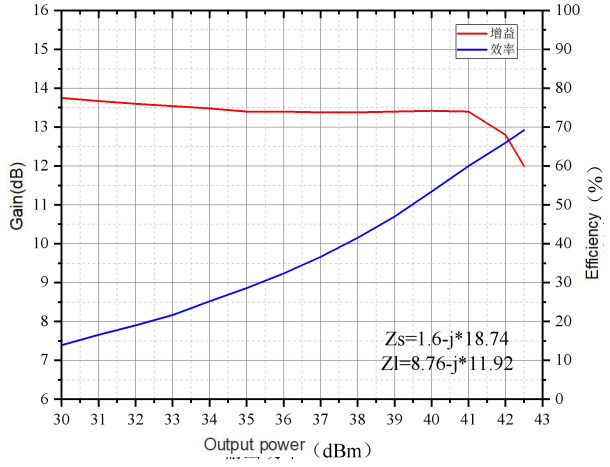
2GHz Gain, Efficiency vs. P_{out}



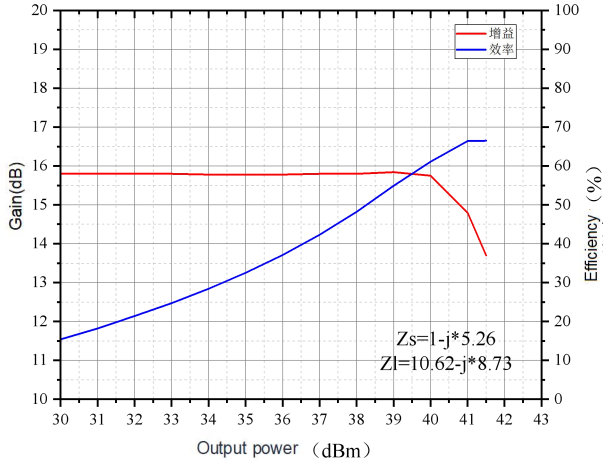
3GHz Gain, Efficiency vs. P_{out}



4GHz Gain, Efficiency vs. P_{out}



5GHz Gain, Efficiency vs. P_{out}



6GHz Gain, Efficiency vs. P_{out}

Typical Performance (Performance measured in Evaluation Board)

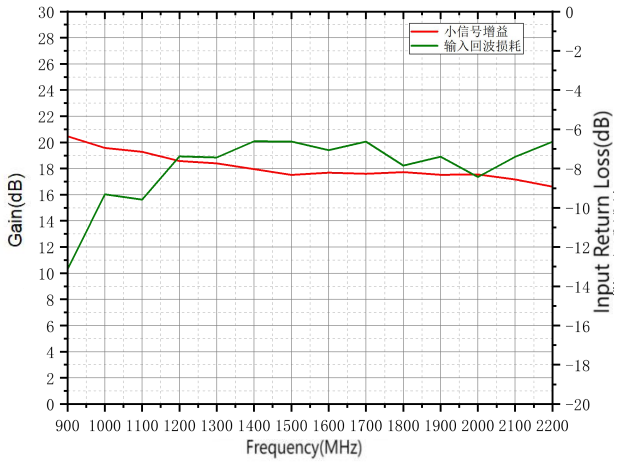
Evaluation Board (0.9GHz ~ 2.2GHz) Test Data							
Parameters	**Typ.**						**Units**
Frequency	900	1000	1300	1500	2000	2200	MHz
Gain	20.5	19.6	18.4	17.5	17.6	16.6	dB
Input Return	-13.1	-9.3	-7.4	-6.6	-8.4	-6.6	dB
Drain Current @P_{sat}	0.93	1.02	1.14	1.18	1.11	0.93	A
Pout (dBm) @P_{sat}	41.4	41.9	42.1	42.0	41.6	41.3	dBm
Pout (dBm) @P_{sat}	13.8	15.5	16.2	15.9	14.5	13.5	W
PAE@P_{sat}	50.7	51.5	47.5	44.2	43.6	47.7	%
Gain @P_{sat}	13.2	13.3	11.8	10.9	12.2	11.1	dB
Test Condition: Temp =25°C, V_{DD}=+28V, I_{DQ}=200mA, CW							

Note: P_{sat} defined as the maximum power output of the evaluation board;

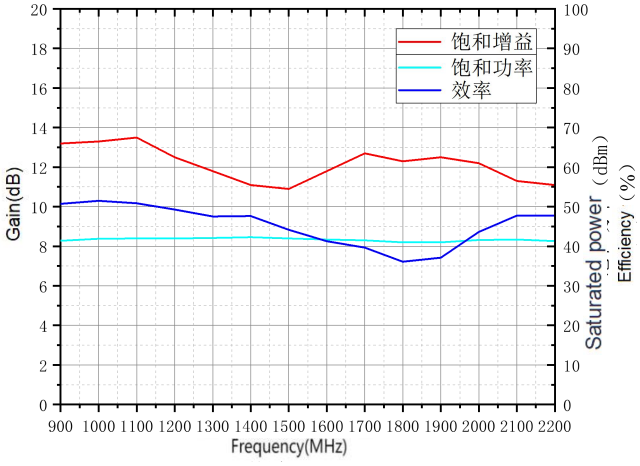
Wide Voltage Characteristics (Evaluation Board Data)

Evaluation Board (0.9GHz ~ 2.0GHz) Test Data					
Parameters	**Typ.**				**Units**
Frequency	900	1200	1600	2000	MHz
Pout (dBm) @P_{sat}	41.9	42.6	42.5	41.3	dBm
Pout (dBm) @P_{sat}	15.4	18.1	17.8	13.5	W
Drain current @P_{sat}	0.91	1.23	1.23	0.92	A
PAE@P_{sat}	53.1	46.0	45.5	45.9	%
Gain @P_{sat}	25.0	19.2	18.1	17.1	dB
Test Conditions: Temp =25°C, =+32V, =200mA, CW ;$V_{DD}I_{DQ}$					

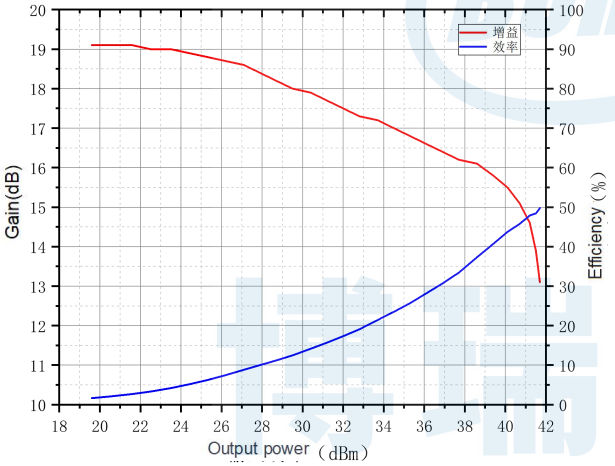
Typical Performance (Evaluation board data: 0.9GHz-2.2GHz, V_{DD}=+28V, I_{DQ}=200mA, Temp=+25℃, CW wave test)



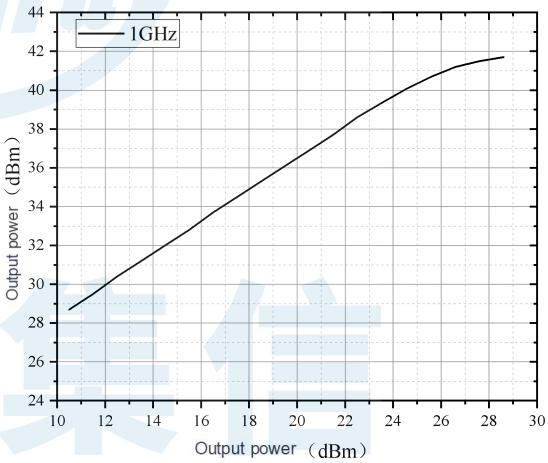
Standing Wave, Gain vs. Freq@25℃



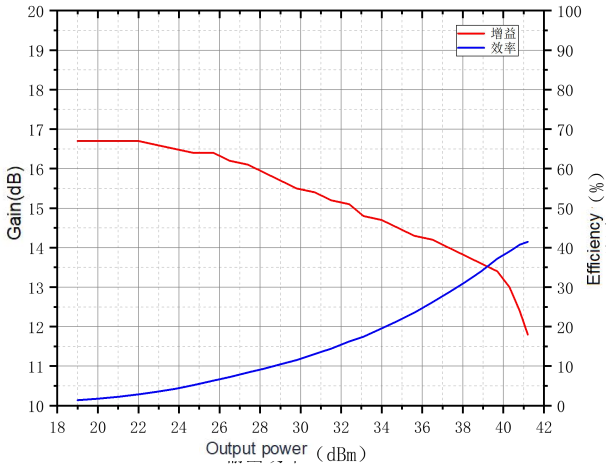
Gain,Saturation Power,Efficiency vs. Freq@25℃



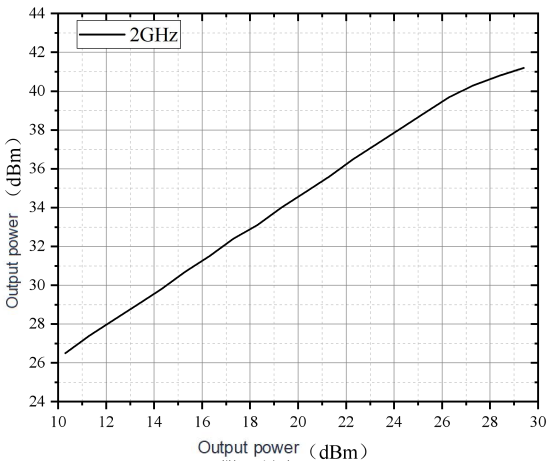
Gain, Efficiency vs. P_{out} @1GHz



P_{out} vs. P_{in}@1GHz

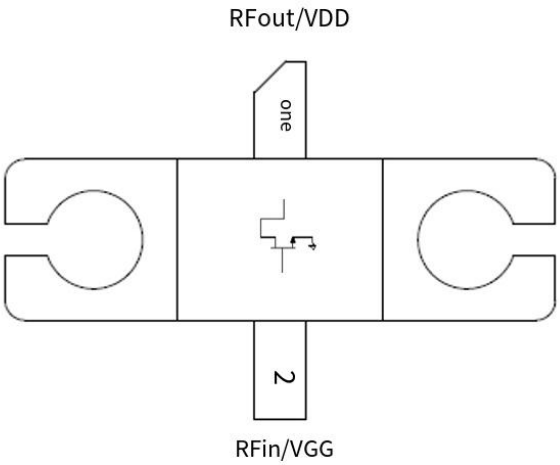


Gain, Efficiency vs. P_{out} @2GHz



P_{out} vs. P_{in}@2GHz

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V_{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 1.5A;

3.Turn on the gate voltage;

4.Turn on drain voltage;

5.Increase the gate voltage (V_{GG}), so that the drain current reaches 200mA;

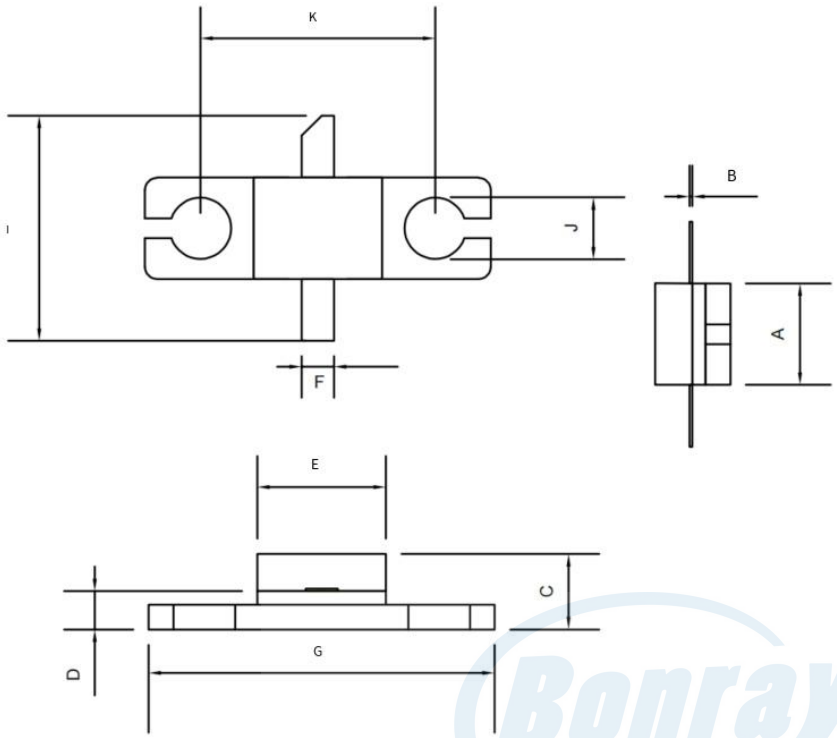
6.Input the RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage;
4. Turn off the gate Supply Voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD Application, gate Supply Voltage decoupling capacitors need to be rigorously evaluated to meet switching speed requirements.

Package Dimensions (mm)



Dim	Units : mm		
	Min	Typ	Max
A	4	4.1	4.2
B	0.05	0.1	0.15
C	2.9	3.15	3.4
D	1.4	1.55	1.7
E	5.05	5.2	5.35
F	1.25	1.3	1.35
G	13.9	14	14.1
H	9.7	10	10.3
J	2.42	2.5	2.58
K	9.45	9.5	9.55

Recommended Soldering Temperature Profile