

Product Features

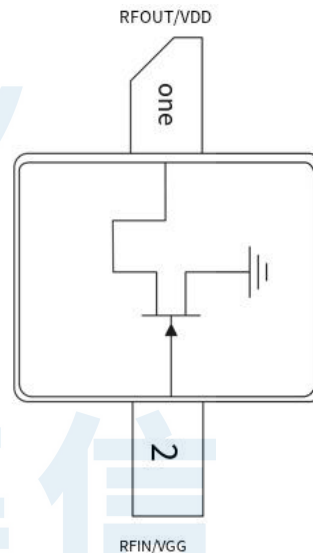
- Frequency: DC ~ 6GHz
- Gain: 17.3dB@900MHz
- Psat: 44.7dBm@900MHz
- PAE: 62.4%(Pout=44.7dBm, 900MHz)
- Operation Voltage: 28V, I_{DQ} 320mA
- Package: PD (ceramic seal)



General Description

The BRGM060025PC is an wideband power amplifier designed using the GaN HEMT process to achieves 20W (44dBm) output in the DC to 6GHz with a power efficiency of 62.4%.The device has the characteristics of high efficiency, high gain and wide bandwidth. This makes the product has a strong application ability in both linear and compressed amplifier circuits, and also simplifies link design and related heat consumption management.

Functional Block Diagram



Applications

- Power Amplification Stage for Wireless Infrastructure
- Test and Measurement Equipment
- Commercial and Military Radars
- Universal Transmitters and Jammers
- Ultrashort Wave Communication Equipment

Ordering Information

Part Number	Package	Description
BRGM060025PD	PD	DC ~ 6GHz 25W GaN Transistor

Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	5.1 A
Gate Current (I_G)	9mA
Continuous Dissipated Power (P_D)	50W
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	245 °C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	320mA (Typ)
Gate Voltage (V_{GG})	-2.52V (Typ)
Channel Temperature (T_{CH})	225 °C (Max)
Continuous Dissipated Power CW (P_D)	42W (Max)
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C ~ +85°C

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions.

Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Conditions: DEMO board test, $T_A = 25^\circ\text{C}$,
 $V_{DD} = +28\text{V}$, $I_{DQ} = 320\text{mA}$, $F_{re} = 1\text{GHz}$, CW wave,
 $P_{out} = 25\text{W}$

Thermal Parameters

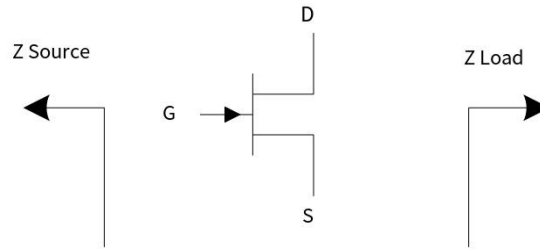
Parameters	Test Condition	Value	Units
Thermal Resistance (θ_{JC})	DC at 85°C case	3.3	$^\circ\text{C}/\text{W}$
Channel Temperature (T_{ch})		225	$^\circ\text{C}$

Note: θ_{JC} to measure the thermal resistance to the bottom of the package;


ESD WARNING


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

博瑞集信

Radio Frequency Features (Load Pull Data)

Optimum Power Matching

Load Pull Data -- Optimal Power Matching							
Parameters	Typ.						Units
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	$2.21 + j * 5.3$	$1.34 * 3.93 j$	$3.48 * 6.53 j$	$2.82 * 13.95 j$	$2.08 * 16.72 j$	$0.15 * 25.65 j$	Ω
Z_{load}	$6.08 * 4.6 j$	$5.79 * 2.4 j$	$5.07 * 5.89 j$	$5.1 * 9.58 j$	$4.24 * 15.86 j$	$14.64 * 20.75 j$	Ω
$I_D @ P_{sat}$	3.13	2.41	2.19	2.8	2.63	2.9	A
Output P_{sat}	47.34	46.15	46.05	47	46.5	47	dBm
PAE @ P_{sat}	60.97	59.9	61.79	64	62	60.8	%
Gain @ P_{sat}	19.13	16.94	12.24	13.6	12.3	10.1	dB

Test Condition: Temp=+25°C, V_{DD} =+28V, I_{DQ} =320mA, CW wave test;

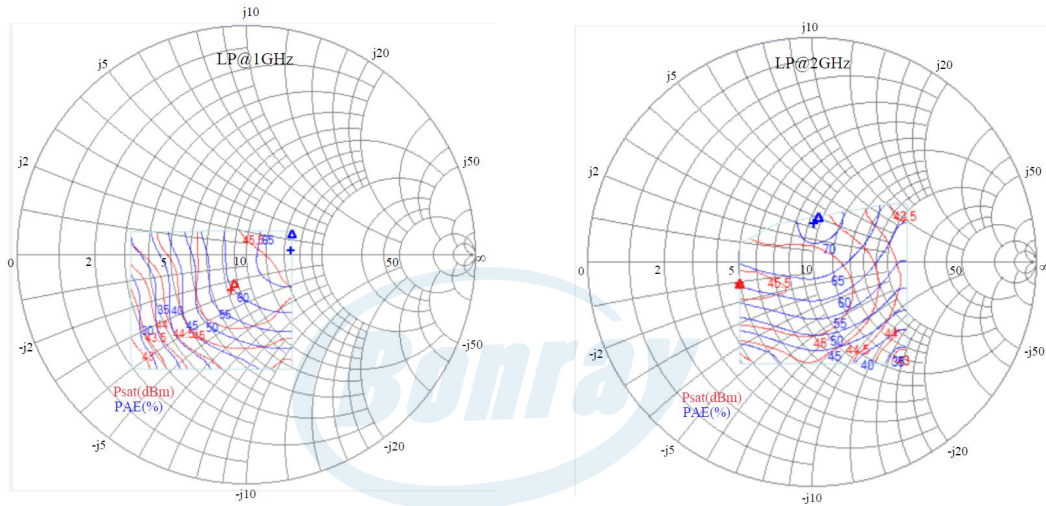
Optimum Efficiency Matching

Load Pull Data -- Best Efficiency Matching							
Parameters	Typ.						Units
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	$2.21 + j * 5.3$	$1.34 * 3.93 j$	$3.48 * 6.53 j$	$2.82 * 13.95 j$	$2.08 * 16.72 j$	$0.15 * 25.65 j$	Ω
Z_{load}	$14.63 + j * 3.08$	$10.44 + j * 5.83$	$4.51 * 3.13 j$	$3.85 * 7.42 j$	$4.2 * 12.76 j$	$14.64 * 20.75 j$	Ω
$I_D @ P_{sat}$	1.55	1.16	1.5	1.22	1.65	2	A
Output P_{sat}	44.88	43.81	44.99	44.06	45.03	46	dBm
PAE @ P_{sat}	70.07	72.32	69.87	74	69.2	66.3	%
Power Gain @ P_{sat}	20.27	16.8	11.76	9.8	10	9.4	dB

Test Condition: Temp =+25°C, V_{DD} =+28V, I_{DQ} =320mA, CW wave test;

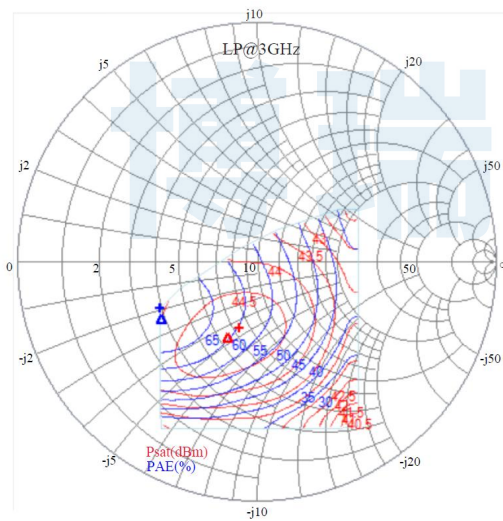
Load Pull Smith

power amplifier typically displays different RF input and output characteristics in a specific impedance environment. due to their own characteristics. The impedance of the device here is the peripheral RF impedance of the amplifier or the impedance of the Load-Pull system rather than the impedance of the amplifier itself. The relevant impedance points can be selected and designed by referring to the contours of Smith circle diagram to ensure the high power and high efficiency of the amplifie



High Impedance Circle Diagram of 1GHz

High Impedance Circle Diagram of 2GHz

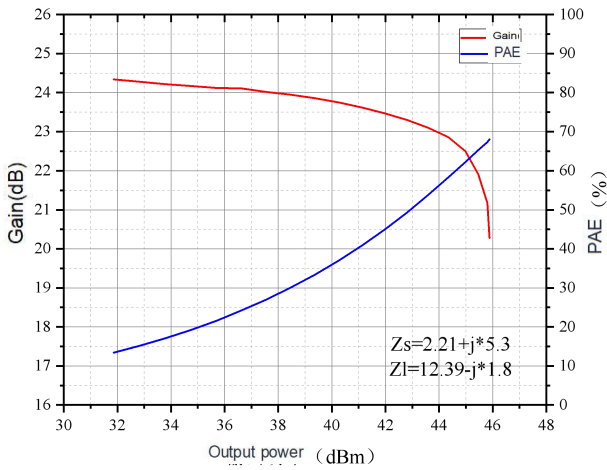


High Impedance Circle Diagram of 3 GHz

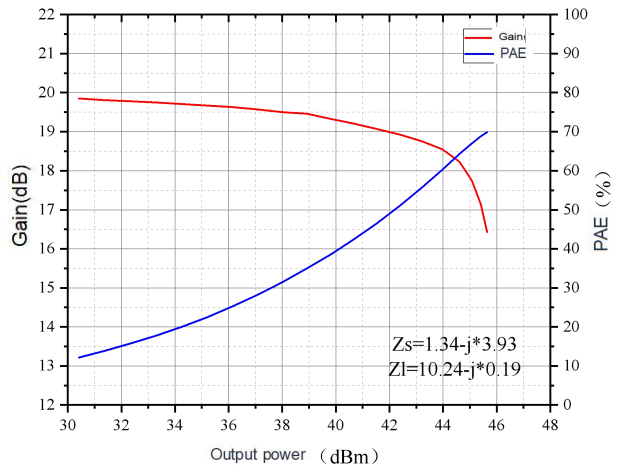
Notes:

1. The central impedance of the Smith circle diagram above is $Z_0=10\Omega$;
2. The contour interval of the red line P_{out} in the Smith circle diagram above is 0.5dB, and the PAE interval is 5%.
3. Test Condition: Temp =+25°C, $V_{DD}=28V$, $I_{DQ}=320mA$, CW wave test;

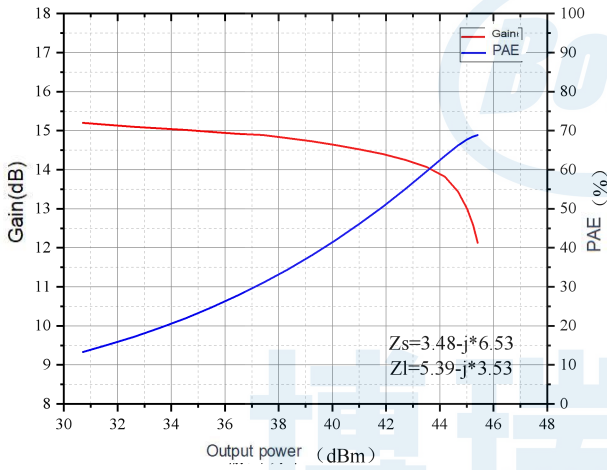
Typical Performance(Load Pull data, Temp =+25°C, V_{DD}=+28V, I_{DQ}=320mA, CW wave test)



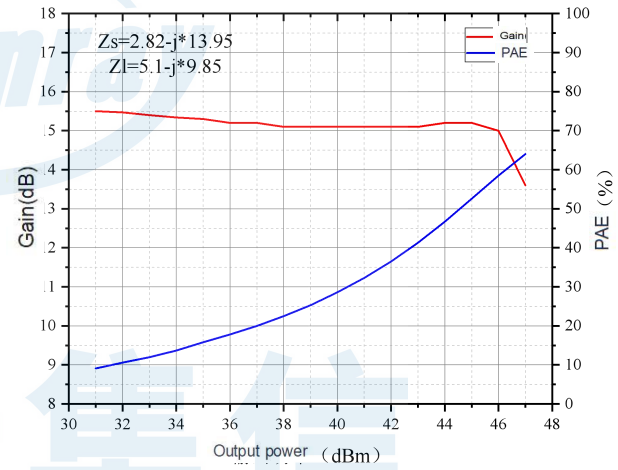
1GHz Gain, PEA vs. P_{out}



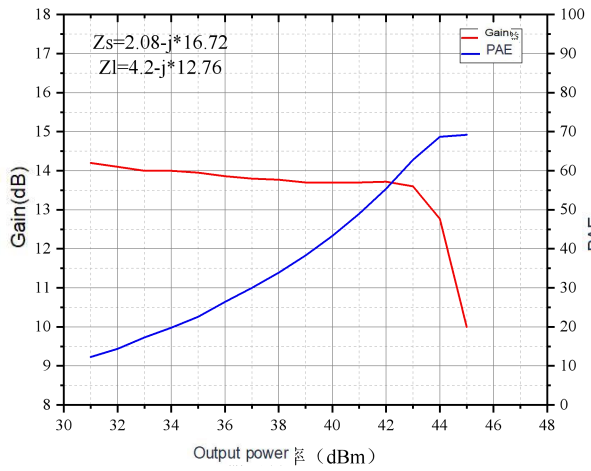
2GHz Gain, PEA vs. P_{out}



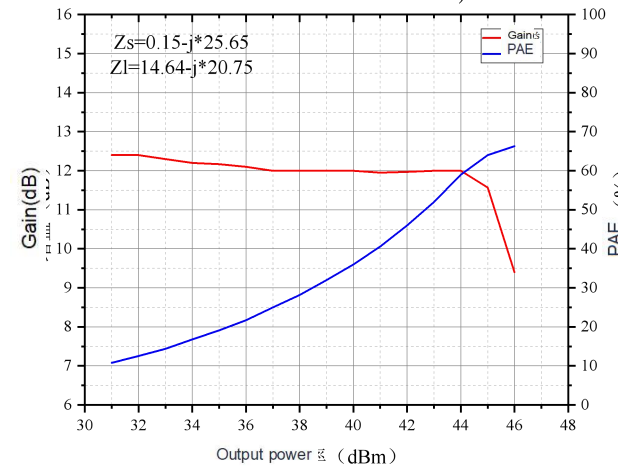
3GHz Gain, PEA vs. P_{out}



4GHz Gain, PEA vs. P_{out}



5GHz Gain, PEA vs. P_{out}



6GHz Gain, PEA vs. P_{out}

Typical Performance (Evaluation board data)

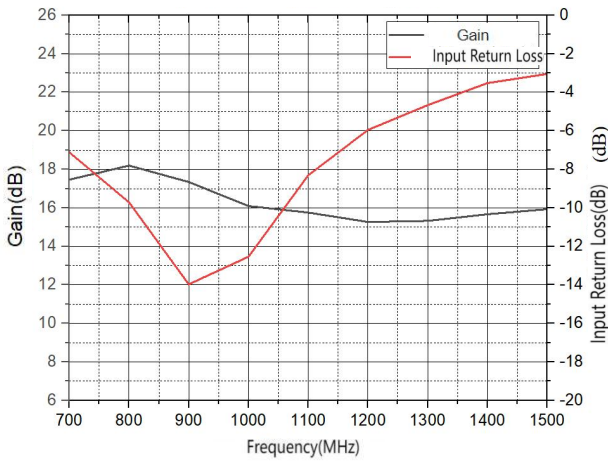
Evaluation Board (0.7GHz ~ 1.5GHz) Test Data										
Parameters	Typ.									Units
	700	800	900	1000	1100	1200	1300	1400	1500	
Frequency	700	800	900	1000	1100	1200	1300	1400	1500	MHz
Gain	17.5	18.2	17.3	16.1	15.8	15.3	15.3	15.7	15.9	dB
Small Signal Input Return Loss	-7.1	-9.7	-14.0	-12.5	-8.3	-6.0	-4.7	-3.5	-3.0	dB
Drain Current @P _{sat}	1.52	1.39	1.58	1.48	1.35	1.36	1.52	1.79	2.03	A
P _{out} (dBm) @P _{sat}	44.7	44.1	44.7	43.9	44.2	43.7	44.4	44.4	44.4	dBm
P _{out} (W) @P _{sat}	29.5	25.7	29.5	24.5	26.3	23.4	27.5	27.5	27.5	W
PAE@P _{sat}	65.6	62.5	62.4	55.6	63.4	56.3	59.6	54.7	48.6	%
Power Gain @P _{sat}	12.6	12.2	12.7	11.9	10.6	10.6	11.3	10.7	11.1	dB
Test Conditions: Temp =+25°C, V _{DD} =+28V, I _{DQ} =320mA, CW										

Note: P_{sat} defined as the maximum power output by the evaluation board;

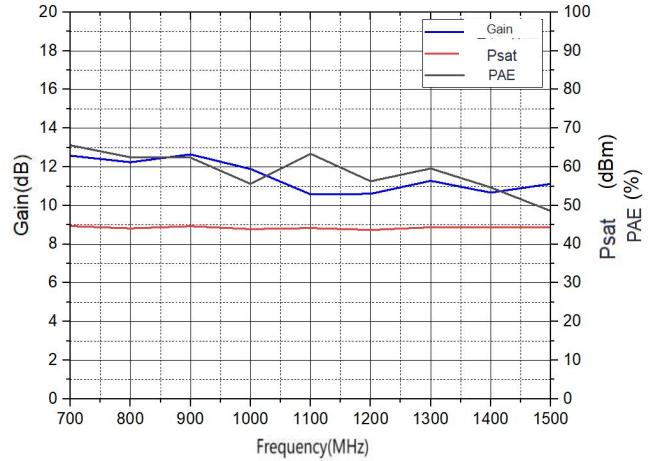
Wide Voltage Characteristics (Evaluation board data)

Evaluation Board (0.7GHz ~ 1.5GHz) Test Data					
Parameters	Typ.				Units
	700	1000	1300	1500	
Frequency	700	1000	1300	1500	MHz
Output Power @P _{sat}	45.8	44.9	45.7	45.5	dBm
Output Power @P _{sat}	38.1	30.8	37.0	35.7	W
Drain Current @P _{sat}	1.79	1.69	1.76	2.25	A
PAE@P _{sat}	66.4	57.1	65.7	49.6	%
Gain @P _{sat}	12.68	11.86	10.61	10.36	dB
Test Conditions: Temp =25°C, V _{DD} =+32V, I _{DQ} =320mA, CW					

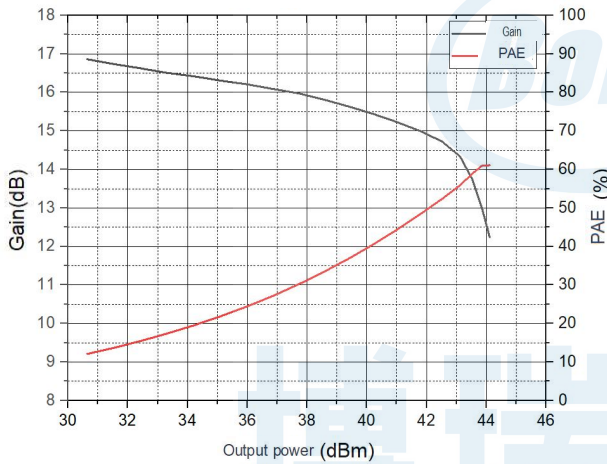
Typical Performance (Evaluation board: 0.7GHz-1.5GHz, Temp =+25°C, $V_{DD}=+28V$, $I_{DQ}320mA$, CW wave test)



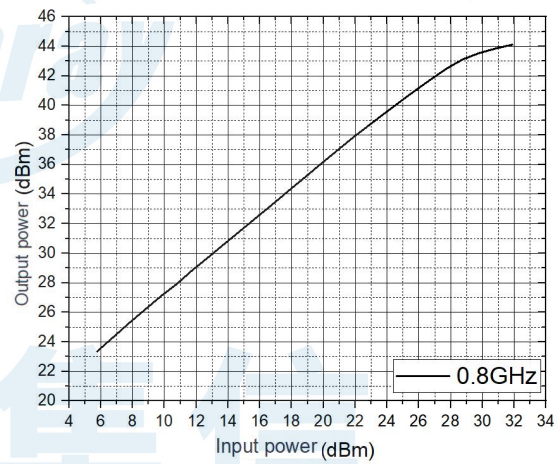
Standing Wave, Gain vs. Freq@25°C



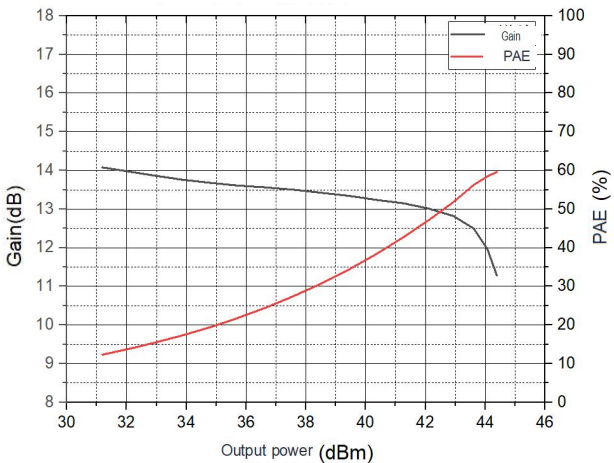
Gain,Psat,PEA vs. Freq@25°C



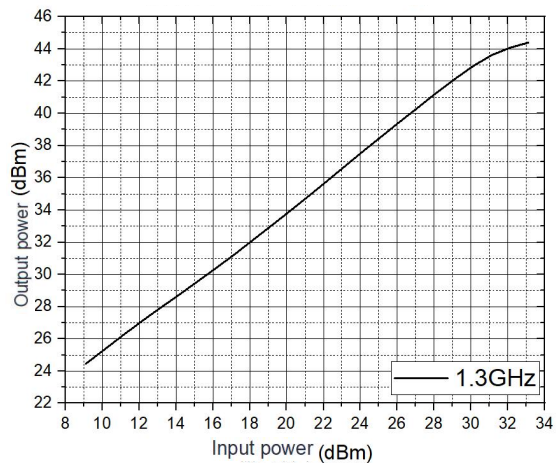
Gain, PEA vs. P_{out}@0.8GHz



P_{out} vs. P_{in}@0.8GHz

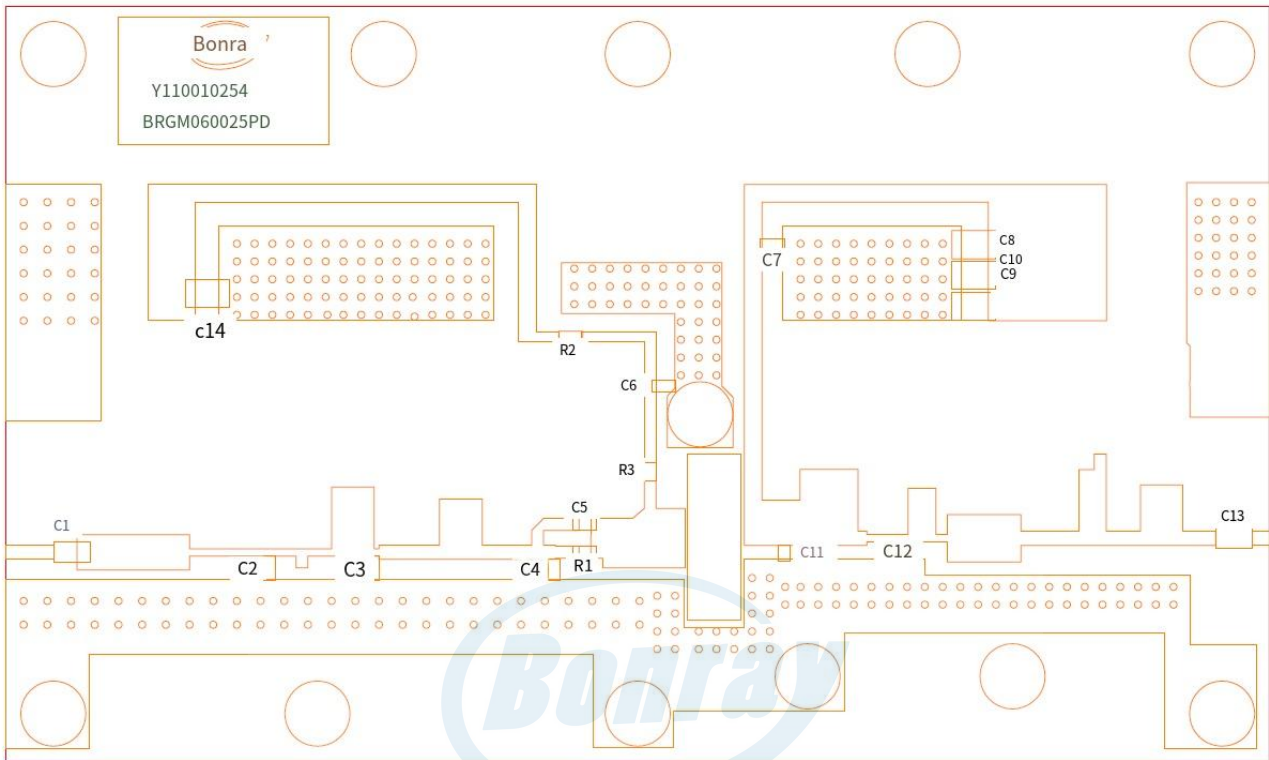


Gain, PEA vs. P_{out}@1.3GHz



P_{out} vs. P_{in}@1.3GHz

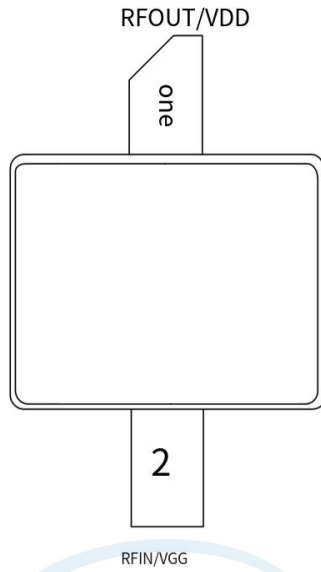
PCB Evaluation Board



Bill of Material

Number	Designator	Description	Package	Quantity
1	C1,C13	CAP,47pF,200VDC,	C1206	2
2	C2	CAP, 1.5 pF, 50 VDC,	C0603	1
3	C3,C4	CAP,4pF,50VDC,	C0603	2
4	C5	CAP, 4.7 pF, 50 VDC,	C0603	1
5	C6	CAP,22pF,50VDC,	C0603	1
6	C7	CAP,47pF,200VDC,	C0805	1
7	C11,C12	CAP, 2.4 pF, 200 VDC,	C0402	2
8	C8,C9,C10,C14	CAP,10uF,200VDC,	C1210	4
9	R1	RES,22Ohm	R0603	1
10	R2	RES,110Ohm	R0603	1
11	R3	RES, 8.2 Ohm	R0603	1

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V _{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V _{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

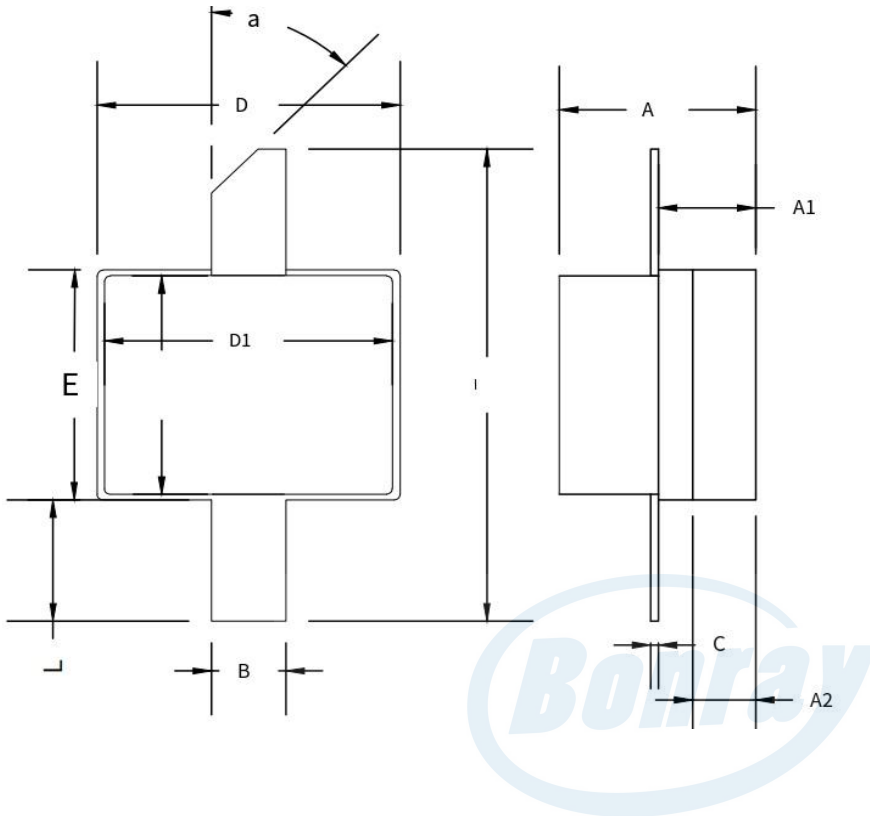
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 5A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 320mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off the drain Supply Voltage voltage;
4. Turn off the gate Supply Voltage voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements

Package Dimensions (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.042	3.195	3.448
A1	1.52	1.57	1.62
A2	0.895	1.020	1.145
B	1.075	1.20	1.325
C	0.115	0.125	0.135
D	4.975	5.100	5.225
D1	4.775	4.900	5.025
E	7.50	8.00	8.50
E1	3.975	4.100	4.225
E2	3.775	3.900	4.025
a	45°		

Recommended Soldering Temperature Profile

