Product Features

Frequency: DC ~ 6GHz

Gain: 17.3dB@0.9GHz

Psat: 44.7dBm@0.9GHz

PAE: Typical value 65%

Operation Voltage: 28V, static current 320mA

Package: PG

Application

Power Amplification Stage for Wireless Infrastructure

Test and Measurement Equipment

Commercial and Military Radars

Universal Transmitters and Jammers

Ultrashort Wave Communication Equipment

General Description

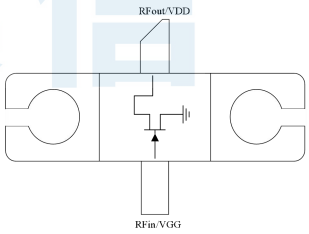
The BRGM060025PG is an wideband power amplifier designed using the GaN HEMT process to achieves 25W (44dBm) output in the DC to 6GHz with a power efficiency of 65%.The power amplifier has the characteristics of high efficiency, high gain and wide bandwidth. This enables the product to have strong Application capabilities in both linear and compressed amplifier circuits, while simplifying link design and related heat consumption management.

The product is packaged in an metal ceramic shell, which is compatible with the BRGM060025PG product package and can meet the needs of high-level application scenarios.

Ordering Information

Part Number	Package	Description
BRGM060025PGG	PG	DC-6GHz 25W GaN Transisor

Functional Block Diagram



Absolute Maximum Ratings

Parameters	Values
Gate Drain Breakdown Voltage (BV_{DG})	100V
Gate Voltage Range (V_{GG})	-6 to 0V
Drain Current (I_D)	5.1 A
Gate Current (I_G)	9mA
Continuous Dissipated Power (P_D)	50W
Channel Temperature (T_{CH})	275 ℃
Mounting Temperature (30 seconds)	245 ℃

Note: Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the deviceat these conditions is not implied. Please pay attention to good heat dissipation under high temperature operation.

Recommended Operating Conditions

Parameters	Numerical values
Drain Voltage (V_{DD})	+28V (Typ)
Drain Static Current (I_{DQ})	320mA (Typ)
Gate Voltage (V_{GG})	-2.52V (Typ)
Channel Temperature (T_{CH})	225 ° C (Max)
Continuous Dissipated Power CW (P_D)	42W (Max)
Storage Temperature	-65℃ ~ +150℃
Operating Temperature	-55℃ ~ +85℃

Note: The electrical specifications of power amplifier tubes are tested under specified test conditions.Electrical performance is not guaranteed when the testspecifications are exceeded.

Impedance mismatch

Markers	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	5:1

Test Condition: DEMO board test, T_A =25℃, V_{DD} =+28V, I_{DQ} =320mA, Fre=1GHz, CW wave, P_{out}=25W

Thermal parameters

Parameters	Test Condition	Value	Units
Thermal resistance (θ_{JC})	Dc bias Test at 85 ° C	3.3	℃/W

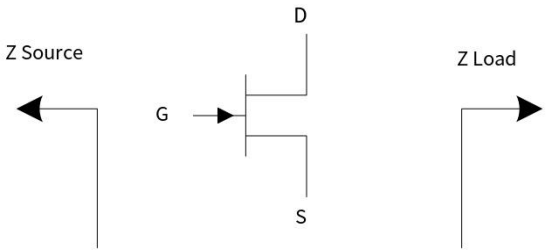
Note: θ_{JC} to measure the thermal resistance to the bottom of the shell;

ESD WARNING

ELECTROSTATIC SENSITIVE DEVICE

OBSERVE HANDLING PRECAUTIONS

Radio Frequency Features (Load Pull Data)



Optimum Power Matching

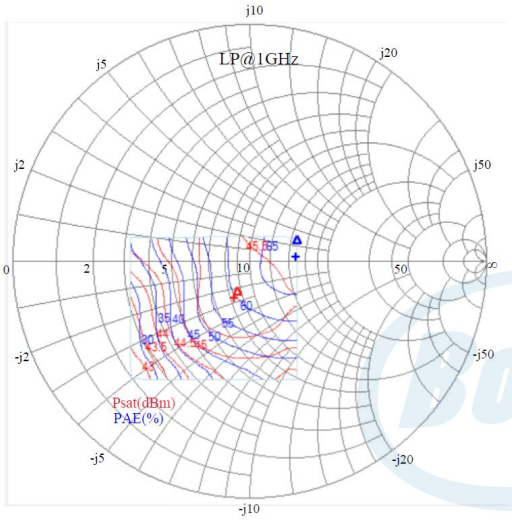
Load Pull Data -- Optimal Power Matching							
Parameters	**Typ.**						**Units**
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	2.21 + j * 5.3	1.34 * 3.93 j	3.48 * 6.53 j	2.82 * 13.95 j	2.08 * 16.72 j	0.15 * 25.65 j	Ω
Z_{load}	6.08 * 4.6 j	5.79 * 2.4 j	5.07 * 5.89 j	5.1 * 9.58 j	4.24 * 15.86 j	14.64 * 20.75 j	Ω
I_D@P_{sat}	3.13	2.41	2.19	2.8	2.63	2.9	A
OutputP_{sat}	47.34	46.15	46.05	47	46.5	47	dBm
PAE@P_{sat}	60.97	59.9	61.79	64	62	60.8	%
Power Gain @P_{sat}	19.13	16.94	12.24	13.6	12.3	10.1	dB
Test Condition: Temp=+25℃, V_{DD}=+28V, I_{DQ}=320mA, CW wave test							

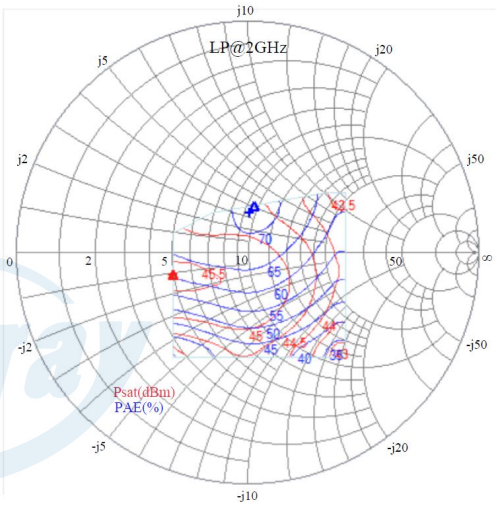
Optimal Efficiency Matching

Load Pull Data -- Best Efficiency Matching							
Parameters	**Typ.**						**Units**
Frequency	1000	2000	3000	4000	5000	6000	MHz
Z_{source}	2.21 + j * 5.3	1.34 * 3.93 j	3.48 * 6.53 j	2.82 * 13.95 j	2.08 * 16.72 j	0.15 * 25.65 j	Ω
Z_{load}	14.63 + j * 3.08	10.44 + j * 5.83	4.51 * 3.13 j	3.85 * 7.42 j	4.2 * 12.76 j	14.64 * 20.75 j	Ω
$I_D@P_{sat}$	1.55	1.16	1.5	1.22	1.65	2	A
$OutputP_{sat}$	44.88	43.81	44.99	44.06	45.03	46	dBm
$PAE@P_{sat}$	70.07	72.32	69.87	74	69.2	66.3	%
Power Gain $@P_{sat}$	20.27	16.8	11.76	9.8	10	9.4	dB
Test Condition: Temp =+25°C, V_{DD}=+28V, I_{DQ}=320mA, CW wave test							

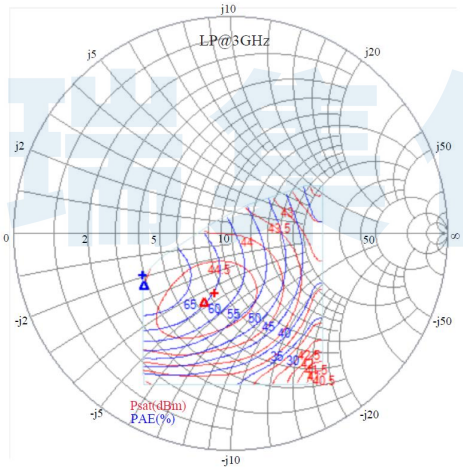
Load Pull Smith

power amplifier typically displays different RF input and output characteristics in a specific impedance environment.due to their own characteristics. The impedance of the device here is the peripheral RF impedance of the amplifier or the impedance of the Load-Pull system rather than the impedance of the amplifier itself. The relevant impedance points can be selected and designed by referring to the contours of Smith circle diagram to ensure the high power and high efficiency of the amplifie





High Impedance Circle Diagram of 1GHz **High Impedance Circle Diagram of 2GHz**

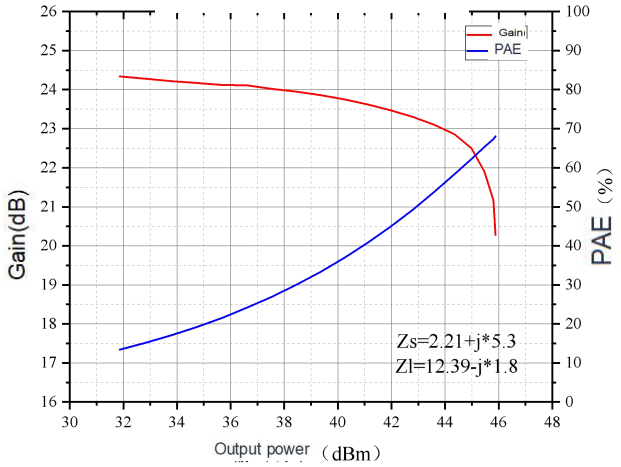


High Impedance Circle Diagram of 3GHz

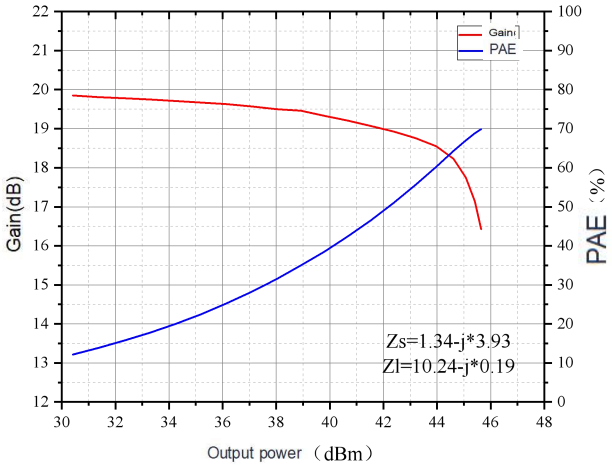
Notes:

1. The central impedance of the Smith circle diagram above is Zo=10Ω;
2. The contour interval of the red line Pout in the Smith circle diagram is 0.5dB, and the PAE interval is 5%;
3. Test Condition: Temp =+25℃, V_{DD}=28V, I_{DQ}=320mA, CW wave test;

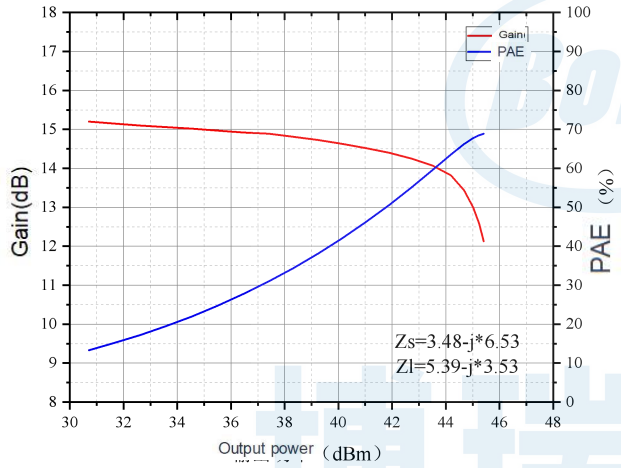
Typical Performance (Load Pull data, Temp =+25℃, V_{DD}=+28V, I_{DQ}=320mA, CW wave test)



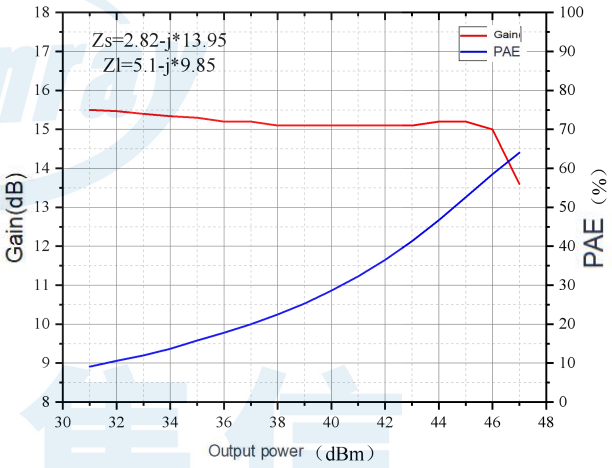
Gain, PEA vs. Pout @1GHz



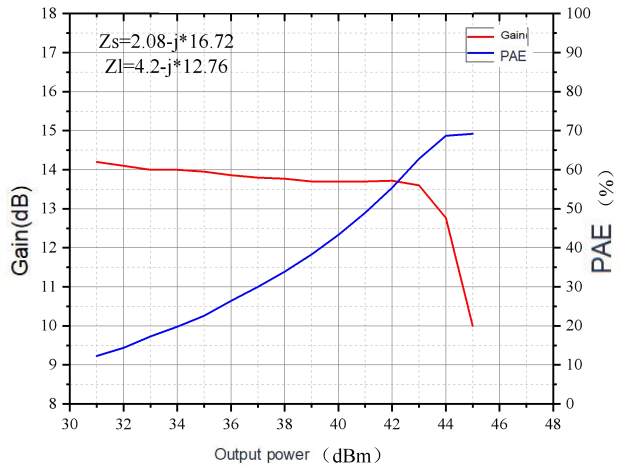
Gain, PEA vs. Pout @2GHz



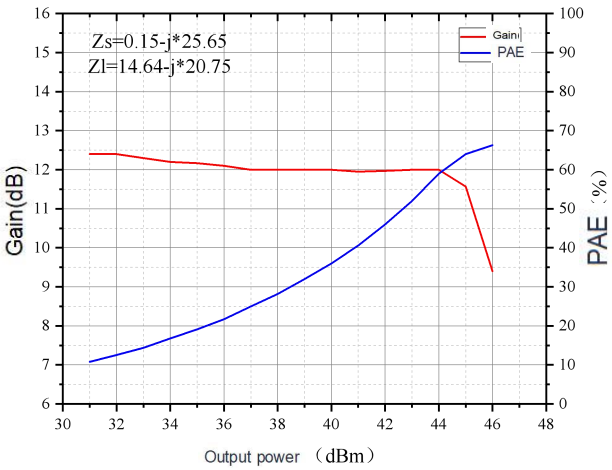
Gain, PEA vs. Pout @3GHz



Gain, PEA vs. Pout @4GHz



Gain, PEA vs. Pout @5GHz



Gain, PEA vs. Pout @6GHz

Typical Performance (Evaluation Board Data)

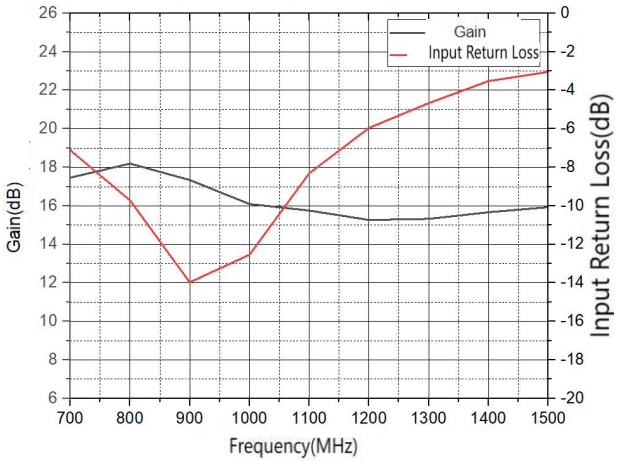
Test Data of Evaluation board (0.7GHz ~ 1.5GHz)										
Parameters	**Typ.**									**Units**
Frequency	700	800	900	1000	1100	1200	1300	1400	1500	MHz
Gain	17.5	18.2	17.3	16.1	15.8	15.3	15.3	15.7	15.9	dB
Small Signal Input Return Loss	-7.1	-9.7	-14.0	-12.5	-8.3	-6.0	-4.7	-3.5	-3.0	dB
Drain Current @Psat	1.52	1.39	1.58	1.48	1.35	1.36	1.52	1.79	2.03	A
Pout (dBm) @Psat	44.7	44.1	44.7	43.9	44.2	43.7	44.4	44.4	44.4	dBm
Pout (dBm) @Psat	29.5	25.7	29.5	24.5	26.3	23.4	27.5	27.5	27.5	W
PAE@Psat	65.6	62.5	62.4	55.6	63.4	56.3	59.6	54.7	48.6	%
Power Gain@Psat	12.6	12.2	12.7	11.9	10.6	10.6	11.3	10.7	11.1	dB
Test Condition: Temp =+25℃, V_{DD}=+28V, I_{DQ}=320mA, CW										

Note: P_{sat} defined as the maximum power output by the evaluation board;

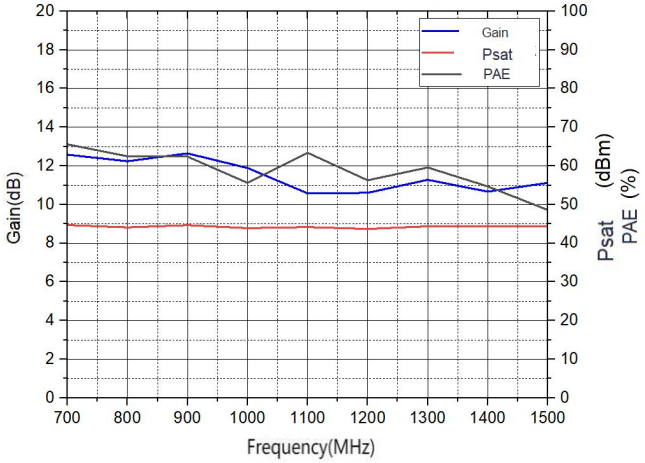
Wide Voltage Characteristics (Evaluation Board Data)

Evaluation Board (0.7GHz ~ 1.5GHz) Test Data					
Parameters	**Typ.**				**Units**
Frequency	700	1000	1300	1500	MHz
Pout (dBm) @P_{sat}	45.8	44.9	45.7	45.5	dBm
Pout (dBm) @P_{sat}	38.1	30.8	37.0	35.7	W
Drain current @P_{sat}	1.79	1.69	1.76	2.25	A
PAE@P_{sat}	66.4	57.1	65.7	49.6	%
Power Gain@P_{sat}	12.68	11.86	10.61	10.36	dB
Test Condition: Temp =25℃, V_{DD}=+32V, I_{DQ}=320mA, CW;					

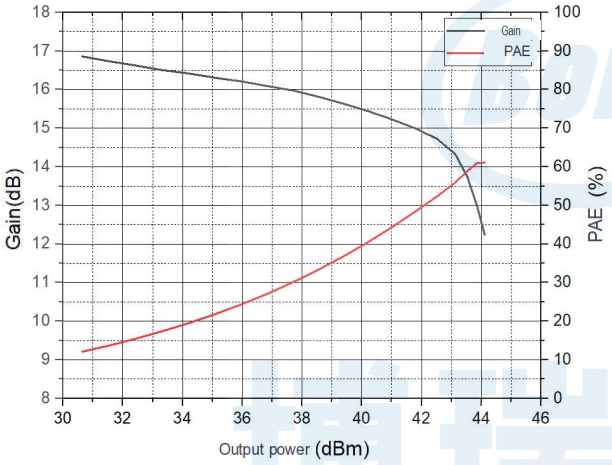
Typical Performance (Evaluation Board: 0.7GHz-1.5GHz, Temp =+25℃, V_{DD}=+28V, I_{DQ}=320mA, CW)



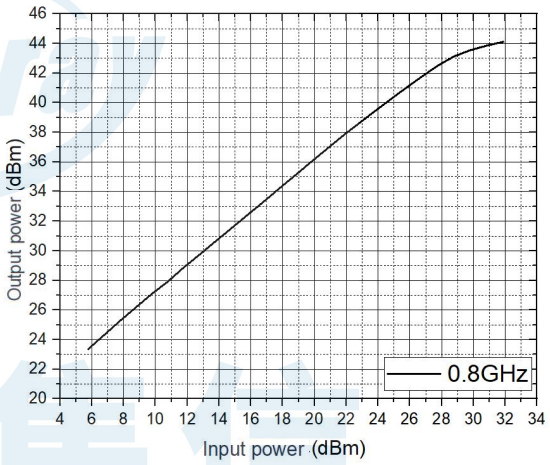
Standing Wave, Gain vs. Freq@25℃



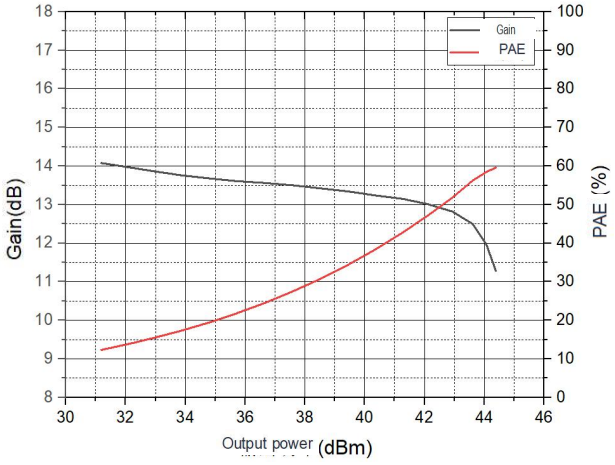
Gain,Psat,PEA vs. Freq@25℃



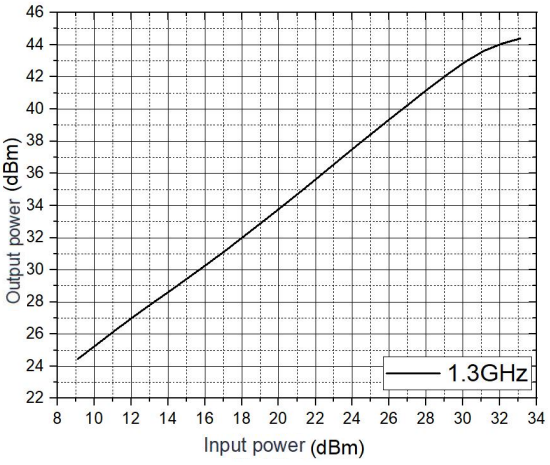
Gain, PEA vs. P_{out} @0.8GHz



P_{out} vs. P_{in} @0.8GHz

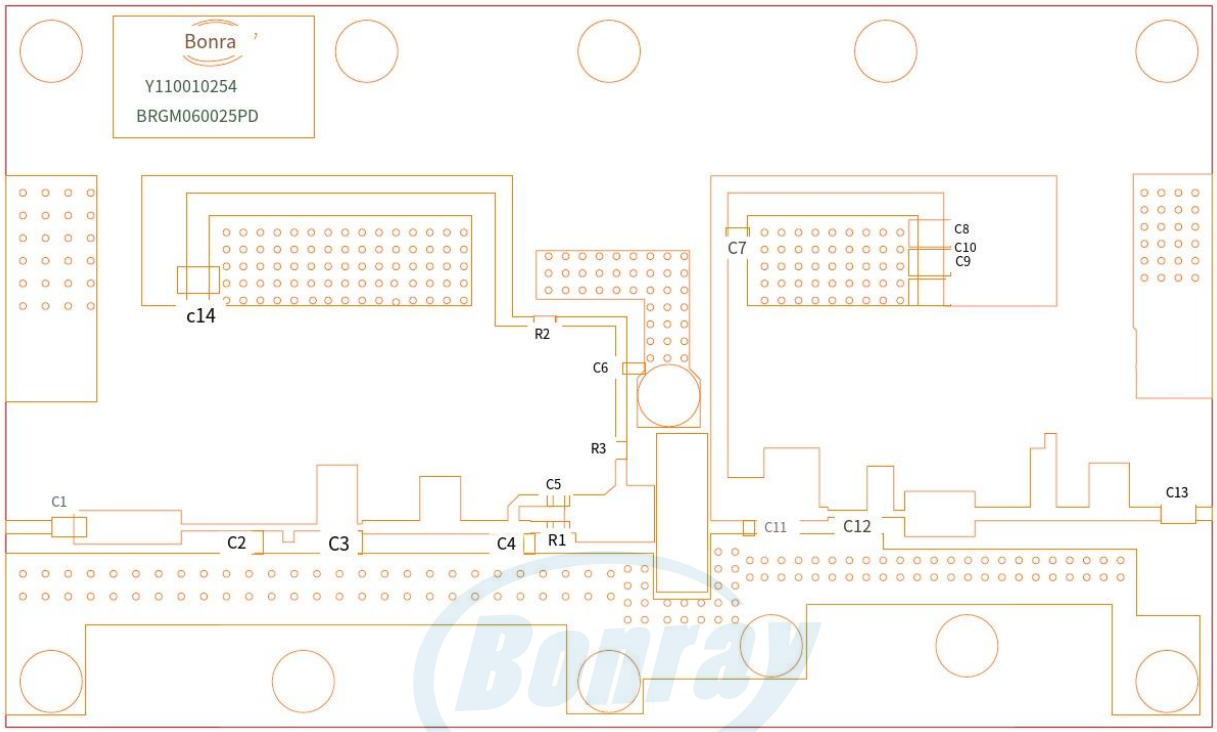


Gain, PEA vs. P_{out} @1.3GHz



P_{out} vs. P_{in}@1.3GHz

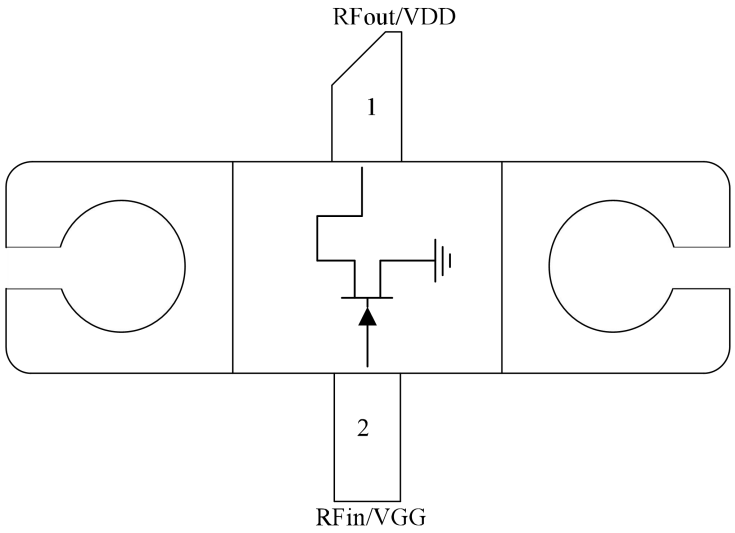
PCB Evaluation Board



Bill of Material

Number	Designator	Description	Package	Quantity
1	C1,C13	CAP,47pF,200VDC,	C1206	2
2	C2	CAP, 1.5 pF, 50 VDC,	C0603	1
3	C3,C4	CAP,4pF,50VDC,	C0603	2
4	C5	CAP, 4.7 pF, 50 VDC,	C0603	1
5	C6	CAP,22pF,50VDC,	C0603	1
6	C7	CAP,47pF,200VDC,	C0805	1
7	C11,C12	CAP, 2.4 pF, 200 VDC,	C0402	2
8	C8,C9,C10,C14	CAP,10uF,200VDC,	C1210	4
9	R1	RES,22Ohm	R0603	1
10	R2	RES,110Ohm	R0603	1
11	R3	RES, 8.2 Ohm	R0603	1

Pin Configuration and Description



Pin Number	Pin Name	Description
1	RFout/V_{DD}	Drain voltage / RF Output matched to 50 ohms;
2	RFin/V_{GG}	Gate voltage / RF Input matched to 50 ohms;
-	Package Base	Source connected to ground;

Power-on Sequence

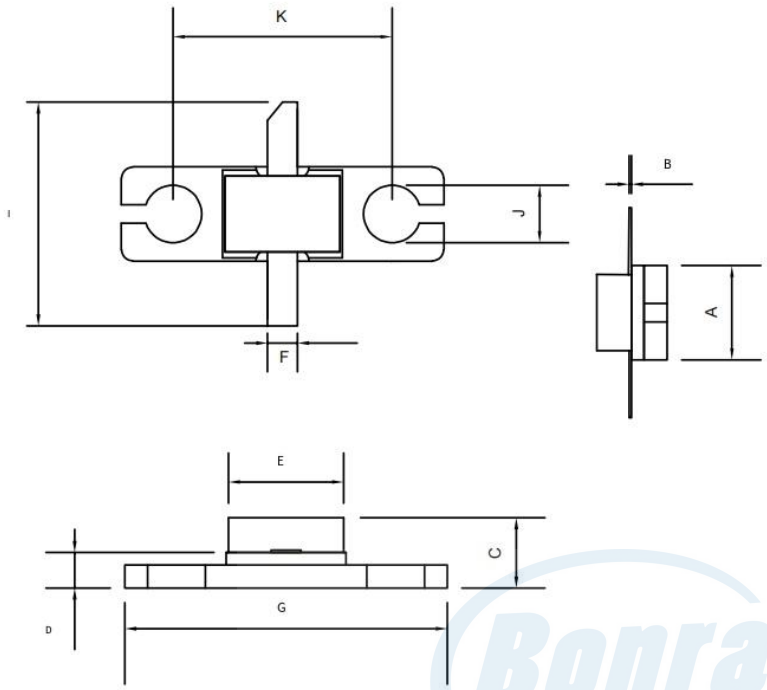
1. Set the gate voltage (V_{GG}) to -5V;
2. Set drain voltage (V_{DD}) to +28V, current limit 5A;
3. Turn on the gate voltage;
4. Turn on drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 320mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the gate Supply Voltage voltage;
2. Turn off the RF signal;
3. Reduce the gate voltage (V_{GG}) to -5V;
4. Turn off the drain Supply Voltage voltage;

Note: In circuit design, bias voltage under-voltage protection is needed with timing protection circuits to ensure that V_{GG} is fully powered up before V_{DD} is applied, and that V_{DD} is lowered to below 5V before V_{GG} is powered down, especially in T_{DD} applications. The gate driving decoupling capacitor needs to be carefully evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Dim	Units : mm		
	Min	Typ	Max
A	4	4.1	4.2
B	0.05	0.1	0.15
C	2.7	2.95	3.2
D	1.4	1.55	1.7
E	4.85	5	5.15
F	1.25	1.3	1.35
G	13.9	14	14.1
H	9.7	10	10.3
J	2.42	2.5	2.58
K	9.45	9.5	9.55

Recommended Soldering Temperature Profile