Product Features

Frequency: DC ~ 2.5GHz

Gain: 16.4dB@1.3GHz

Psat (dBm): 52.7dBm@1.3GHz

PAE: 61%(Pout=52.7dBm@1.3GHz)

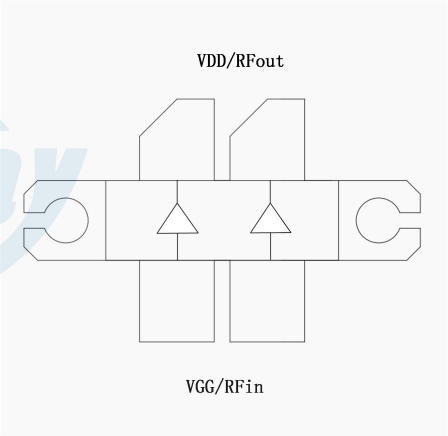
V_{DD}Power Supply 28V, I_{DQ} 450mA

Package: PN (ceramic seal)

General Description

The BRGM025250PC is a pre-matched transistor designed using the GaN HEMT process, using a +28V drain supply to achieves 250W(53.9dBm) output in the DC to 2.5GHz with a power added efficiency (PAE) up to 61%. The power amplifier has the characteristics of high efficiency, high gain and wide bandwidth, which makes the product has strong application capabilities in both linear and compressed amplifier circuits, while also simplifying link design and related heat consumption management.

Functional Block Diagram



Ordering Information

Part Number	Package	Description
BRGP025250PND	PN	DC ~ 2.5GHz GaN Transistor

Absolute Maximum Ratings

Parameters	values
Gate drain breakdown voltage (BV_{DG})	100V
Gate voltage range (V_{GG})	-6 to 0V
Drain current (I_D)	34A
Gate current (I_G)	60mA
Continuous dissipated power (P_D)	280W
Channel temperature (T_{CH})	225 ℃
Mounting temperature (30 seconds)	245 ℃

Note: Operation of the device outside the parameter ranges given absolute-maximum-ratings conditions may cause permanent damage, and. exposure to absolute-maximum-ratings conditions for extended periods will affect the reliability. Under high temperature operation, please pay attention to good Dissipate heat.

Recommended Working Conditions

Parameters	values
Drain voltage (V_{DD})	+28V (Typ)
Drain static current (I_{DQ})	450mA (Typ)
Gate voltage (V_{GG})	-2.5V (Typ)
Channel temperature (T_{CH})	225 ° C (Max)
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ to +85℃

Note: The power amplifier tube electrical specifications are tested under the specified Test Condition. Electrical performance is not guaranteed when the test specifications are exceeded.

Impedance Mismatch

Signs	Parameters	Typ.
VSWR	Impedance Mismatch Ruggedness	TBD

Test Condition: DEMO board test, =T_A25℃, V_{DD}=+28V, I_{DQ}=450mA, Freq=1GHz, CW wave, =P_{out}100W;

Thermal Parameters

Parameters	Test Condition	value	Units
Thermal resistance (θ_{JC})	DC at 85 ° C case	TBD	℃/W
Channel temperature (T_{ch})		225	℃

Note: θ_{JC} to measure the thermal resistance to the bottom of the package

ESD Warnings

ELECTROSTATIC SENSITIVE DEVICE

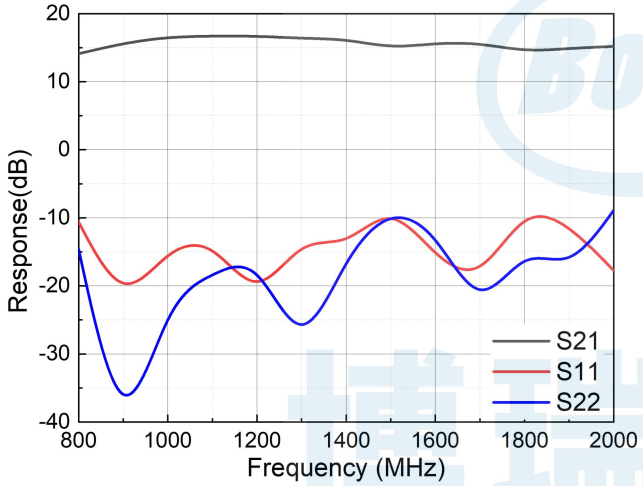
OBSERVE HANDLING PRECAUTIONS

Radio Frequency Features(EVB test data, 0.8GHz~2GHz)

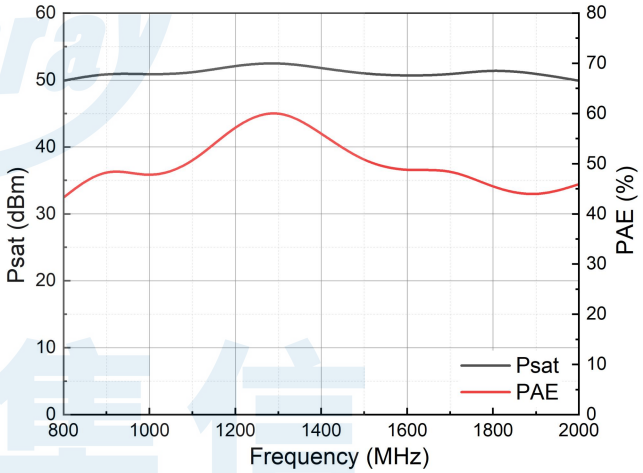
Parameters	Typ.											Units
Frequency	800	1000	1200	1300	1400	1500	1600	1700	1800	1900	2000	MHz
Gain	14.12	16.46	16.66	16.40	16.07	15.26	15.56	15.48	14.71	14.86	15.19	dB
Small Signal Input Return	-10.62	-15.60	-19.38	-14.62	-13.04	-10.11	-15.11	-17.10	-10.53	-11.61	-17.74	dB
Drain Current @P_{sat}	7.26	8.66	9.73	10.25	8.99	8.10	7.81	8.00	10.35	9.50	6.97	A
Pout (dBm) @P_{sat}	49.9	50.8	52.2	52.7	51.8	50.9	50.6	50.8	51.6	51.0	49.9	dBm
Power Gain @P_{sat}	10.0	12.5	13.1	12.8	11.7	11.2	11.0	10.8	10.2	10.6	10.8	dB
PAE@P_{sat}	43.24	46.79	57.90	61.48	56.07	50.13	48.33	49.21	45.11	43.21	45.91	%

Test Condition: Temp =+25℃CV_{DD}, =+28V, =I_{DQ}450mA, CW ;

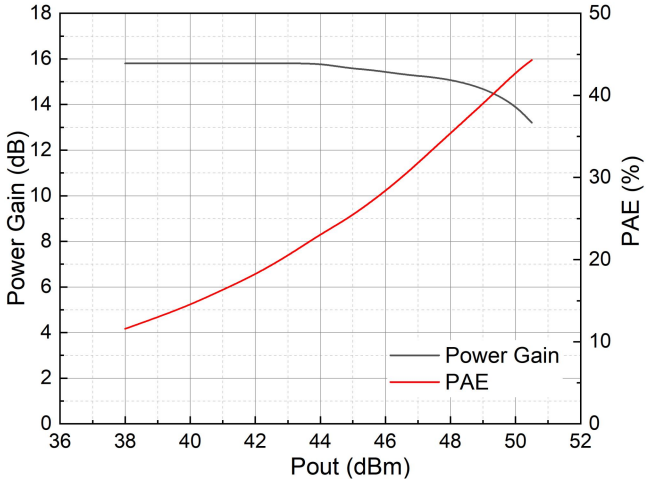
Note: defined as the saturation power output of the evaluation boardP_{sat}.



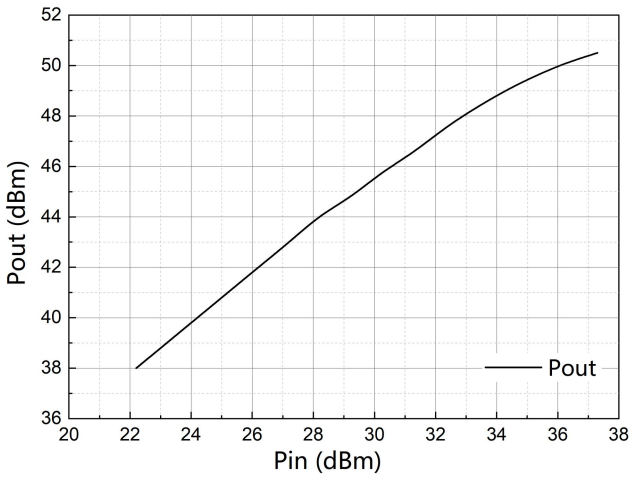
Gain, Output Return, Input Return vs. Freq



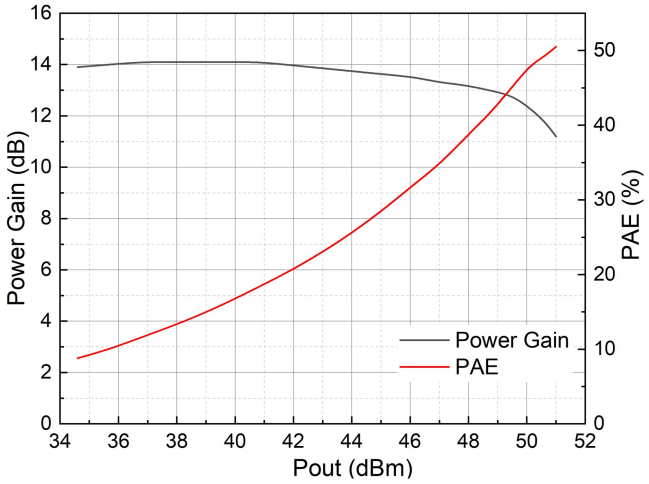
Saturated Pout & Added Efficiency vs. Freq



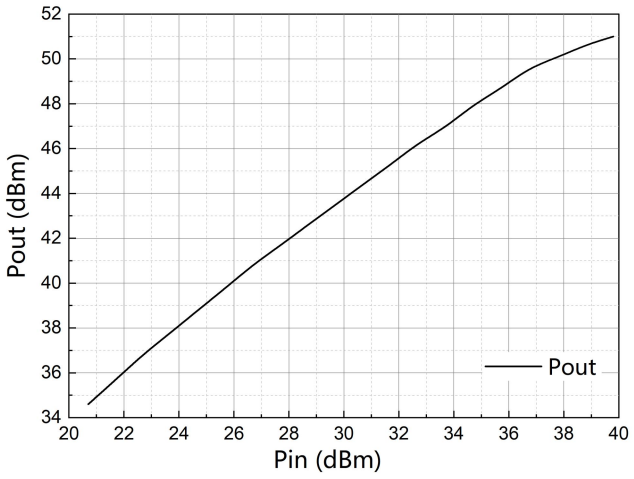
Gain & Added Efficiency vs. P_{out} @1GHz



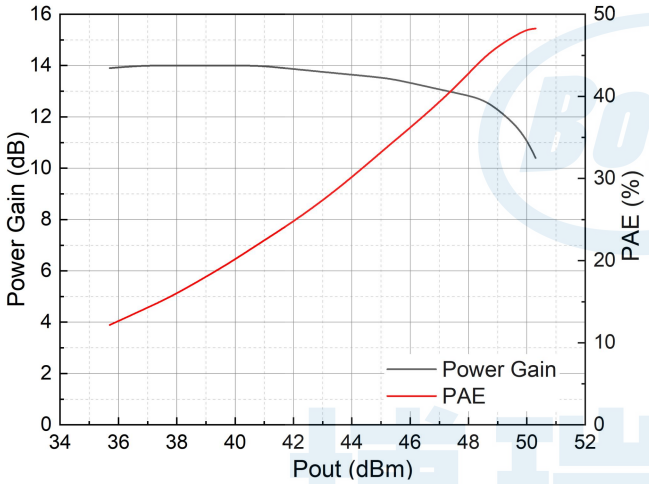
P_{out} vs. P_{in} @1GHz



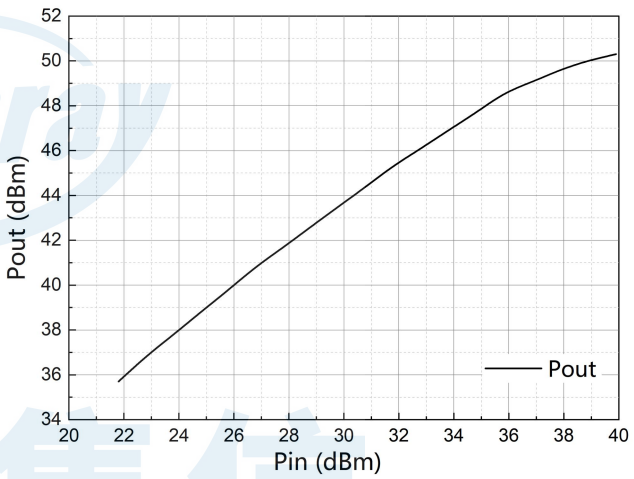
Gain & Added Efficiency vs. P_{out} @1.5GHz



P_{out} vs. P_{in} @1.5GHz

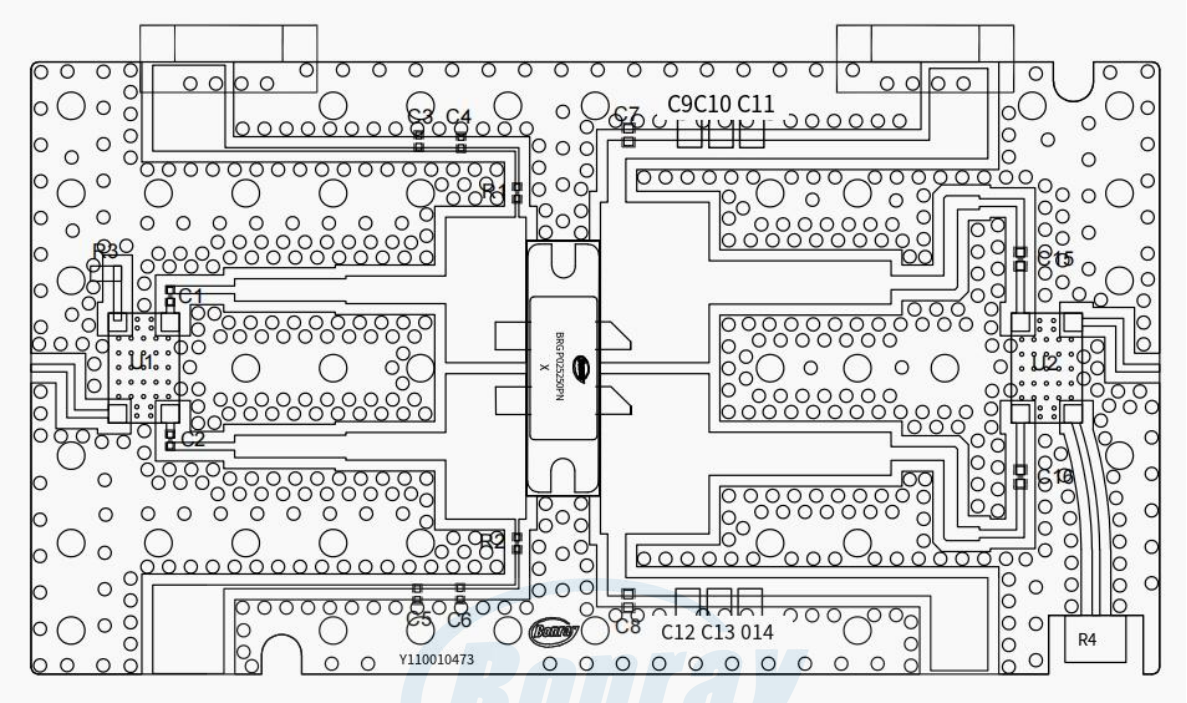


Gain & Added Efficiency vs. P_{out} @2GHz



P_{out} vs. P_{in} @2GHz

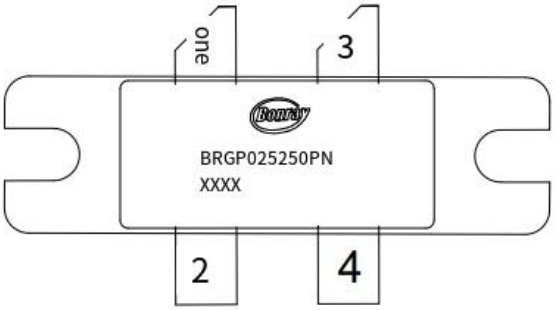
Typical Application Schematic



Bill of Material

Reference Designator	Package Size	Value	P/N
C1, C2, C4, C6, C15, C16	0603	20pF	GQM1875C2E200GB12D
C3, C5	1210	47uF	GRM32ER61C476KE15L
C7, C8	0805	100pF	VJ0805D101JXPAJ
R3	5 mm * 2.5 mm	50 Ω	RFR50-20CT0421B
R1, R2	0603	51 Ω	RC0603FR-0751R1L
R4	9mm*6mm	RFT50-150TM0906	RFT50-150TM0906
U1, U2	/	3dB bridge	HC1650W03
C9, C10, C11, C12, C13, C14	1210	10uF	GRM32EC72A106KE05#
C17, C18	8mm*12mm	100uF 50V electrolytic capacitor	CHONGX 8X12

Pin Configuration and Description



Pin Number	Pin Name	Description
1, 3	RFout/V_{DD}	Drain, drain voltage input, RF power signal 50Ω system output;
2, 4	RFin/V_{GG}	Gate, gate voltage regulation, RF signal 50Ω system input;
-	Package Base	Ground substrate, which needs to be welded to the substrate under the card opening window;

Power-on Sequence

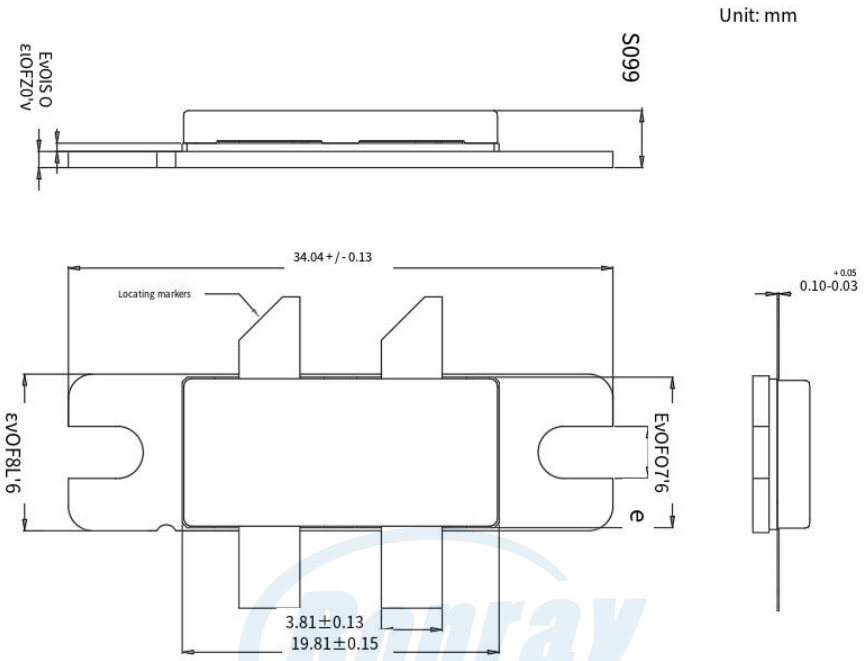
1. Set the gate voltage (V_{GG}) to -5V
2. Set drain voltage (V_{DD}) to +28V, current limit 15A;
3. Turn on the gate voltage;
4. Open drain voltage;
5. Increase the gate voltage (V_{GG}) so that the drain current is 450mA;
6. Input RF signal;

Power-off Sequence

1. Turn off the RF signal;
2. Reduce the gate voltage (V_{GG}) to -5V;
3. Turn off drain supply voltage;
4. Turn off the gate supply voltage;

Note: When the circuit is designed, the offset voltage needs to have a timing protection circuit to ensure that it is fully powered on before adding, and ensure that it is reduced to below 5V when powering off, before starting to power off; $V_{GG}V_{DD}V_{DD}V_{GG}$Especially in TDD applications, gate supply decoupling capacitors need to be rigorously evaluated to meet the switching speed requirements.

Package Dimensions (mm)



Recommended Soldering Temperature Profile